

The invention relates to a circuit arrangement for the recognition and/or monitoring of synchronising words contained in a serial data stream in accordance with the first part of claim 1. Such a circuit arrangement is known from US-A-4 607 378.

For the data processing in respect of the serial transmission of digital signals which are arranged in a predefined frame structure, it is known to utilise a data processor which carries out programme controlled calculations. Associated items of data are identified by control signals which are produced by means of a circuit arrangement with the aid of synchronising words contained in the data stream.

The general aim is to integrate circuit arrangements of this type together with others in order to thereby reduce the necessary number of individual parts, to diminish the size of the assembly and to increase the reliability of the circuit arrangement. However, the dimensions of the chip surface on which the component groups can be integrated is limited. Consequently it is a matter of importance to utilise the available space particularly sparingly.

Bearing in mind the dimensionally limited surface of the chip in a highly integrated circuit, the object of the invention is to develop a circuit arrangement which enables a reliable recognition and/or monitoring of synchronising words contained in a serial data stream with the least possible outlay, in particular as regards flip-flop stages.

This object is achieved in a circuit arrangement in accordance with the first part of claim 1 by the features mentioned in the characterising part.

For the checking of the synchronising words present in the data stream, the circuit arrangement in accordance with the invention restricts itself to the storage cells present in a shift register and on each occasion only compares the data items occurring in these storage cells. If a data combination instantaneously corresponds to a synchronising word, then a first recognition or monitoring signal appears for a short time at the output of the logical element due to the logical AND gating. Thus, the circuit arrangement is particularly suited for the first time, to picking out from a data stream a combination which could correspond to a synchronising word.

If the synchronising word is longer than the storage cells available in the shift register then the first check can be

restricted initially to a part of the synchronising word. Thereafter, for the evaluation of the remaining places, the same shift register can be loaded with a reference value and the remaining portion of the synchronising word, which, in the interim, is located in the other shift register, can be directly compared bit by bit with the reference value. Thus, the first shift register is doubly utilised whereby there is no delay in the further checking due to the loading of the reference value immediately after the first recognition of a portion of the synchronising word.

Further developments and advantageous embodiments are apparent from the further claims, the description and the drawing which illustrates one embodiment of the invention.

In the drawing:

Fig. 1 shows a circuit diagram embodying the invention as a component part of a receiver for digital satellite broadcasting,

Fig. 2 a pulse diagram for explaining the circuit depicted in Fig. 1.

The receiver for digital satellite broadcasting is provided for receiving radio programmes in accordance with the specification of the radio transmission process in TV-SAT. The interlacing of the programmes into a frame structure and the incorporation of additional programme information in special service frames and special service super frames are described in more detail in the DE-OS 33 08 025.

In the present case, the special service frames SA and the special service super frames SAÜ which are formed from the special service bits transmitted in the main frame A in accordance with the above mentioned specification are of interest. Each special service frame begins with a 16 place synchronising word, which the data words that include items of information regarding the type of programme of the transmitted radio programme follow. Of these however, only the four succeeding data words are occupied by useful items of information, while the data items in the remaining two data words are irrelevant.

The special service super frame SAÜ comprises eight special service frames SA wherein however, the synchronising word for the special service super frame is slightly different from the other synchronising words. Items of information regarding the

type of programme for the programme 1 and the programme 2 are contained in the first special service frame SA of the special service super frame SAÜ.

After switching on or after a loss of synchronisation, the circuit illustrated in Fig. 1 is initially in a search mode. The data stream i.e. the special service bits referenced KB reach a flip-flop 1 which is clocked at a clock rate T32 that has the same frequency as the KB sequence. A shift register 2, which is followed in turn by a shift register 3, is connected to the flip-flop 1. The flip-flop 1 and the shift register 2 may also be combined as partial shift registers in a common shift register 1, 2 having a further storage cell whereby however, the first storage cell is only connected in series and is not loaded with reference values.

Inputs of a logical element 9 are connected to the outputs Q1 to Q8 of the storage cells of the shift register 2. If a data configuration which corresponds to the synchronising word appears at the outputs Q1 to Q8 then a recognition and/or monitoring signal SHL occurs at the output of the AND gate element 9. On the one hand, this triggers off a counting sequence in a control circuit 7, 8 in order to be able to test for a positive recognition of the synchronising word after the expiry of the frame duration and, on the other hand, calls up a load command LD2 which loads a reference value corresponding to a previously occurring portion of the just recognised synchronising word into the shift register 2. Portions of longer synchronising words are still available since the data items leaving the shift register 2 are taken over into the shift register 3. The circuit arrangement is thus also in a position to be able to check synchronising words which have more places than are present in the shift register 2. For checking these places of the synchronising word, the output of the shift register 3 and the output of the shift register 2, the latter via a logic element 15, are connected to an EXCLUSIVE-OR gating element 16. A logical L appears at the latter's output upon equality of the bits of the reference value and the actual value stored in the shift register 3 and a logical H for non-equality.

This signal reaches an error counter 4 via a gating element 12 which is clocked at the clock rate T32N and from there, after a scan command SYSU emitted by the control circuit 8 in the "search" mode and SYLF in the "monitoring" mode, it reaches a shift register 5 that retains the consecutive number of synchronising words which are not present or are in error. An evaluating matrix 6 connected to an output of the shift register 5 determines when to switch from a "monitoring" mode to a

"search" mode or when to switch back from the latter to the "monitoring" mode during the recognition or monitoring of synchronising words.

If a synchronising word is correctly identified immediately after switching on, then the logical level of SU at the output of the evaluating matrix 6 is changed i.e. the "search" mode comes to an end. After a time point determined by the counter 7 which occurs immediately before the arrival of a synchronising word, reference values are accepted into the shift registers 2 and 3 by means of a loading command LDU appearing thereat as LD1. A comparison is now immediately made with the first bit of the synchronising word in that the arriving data items are fed via a gating element 15 to the one input of the EXCLUSIVE-OR gating element 16 while the reference values read out from the shift register 3 are present on the other input. Thereafter, a bit by bit comparison is effected whereby possible errors are stored in turn in the error counter 4.

Originally, the shift register 3 is used for other purposes, namely, for the transmission of data into a connected data processor. It is particularly advantageous in this case that irrelevant data items that do not have to be processed by the connected data processor are transmitted in the data stream in accordance with the above-mentioned specification before the arrival of the synchronising word. Consequently, it is possible to interrupt the acceptance of data into the data processor and to let the complete reference value of the expected synchronising word into the shift registers 2 and 3 instead, whereby the first portion in time is accepted into the shift register 3 and the second portion in time into the shift register 2.

The recognition of the synchronising words which in each case precede the special service super frames gives rise to yet another problem. These differ from the other synchronising words in that the 11th and 12th places have another logical condition. In order not to set the error counter 4 in this case, the arriving synchronising word is in each case converted such that it corresponds to the frequently occurring synchronising word. This means, the frequently occurring synchronising word is not changed and the frequently occurring synchronising word is formed from the rarely occurring synchronising word having the altered 11th and 12th places. It is ensured in this manner that the different synchronising words are dealt with in the same way and are not denoted as errors.

The data modifying circuit serving this purpose comprises two EXCLUSIVE-OR gating elements 17 and 18 of which the first is arranged between the D input and the Q output of the flip-flop 1 and the second between the Q output of the flip-flop 1 and the Q1 output of the flip-flop 2. The outputs of the EXCLUSIVE-OR gating elements 17 and 18 are connected to the outputs of the control matrix 8 at which interrogation signals ABF1 and ABF2 are produced at the times at which the 11th and 12th places of the synchronising word appear. Hereby, a consistent logical condition is produced at the output of the gating element 20d independently of the logical condition of the places insofar as the 11th and 12th places have equal polarities.

New Claim 1

1. Circuit arrangement for the recognition and/or monitoring of synchronising words contained in a serial data stream, wherein the circuit arrangement has a first shift register into which the data stream is continuously written, characterised in that, outputs (Q1, Q8) of the storage cells of the first shift register (1, 2) are connected by a logical AND element (9) at whose output a recognition or monitoring signal (SHL) appears, that a second shift register (3), into which the data stream read out from the first shift register (1, 2) is written, is connected downstream of the first shift register (1, 2), that a first reference value is loaded into the first partial shift register (2) by the recognition signal (SHL) from the AND element (9) and that the outputs of the first (1, 2) and second shift register (3) are connected by a logical combining element (16) at whose output a second recognition signal or monitoring signal appears.

2. Circuit arrangement in accordance with Claim 1, characterised in that, the control circuit contains a counter (7) which is set to a starting value by the first recognition signal, that a switching signal (LDU) in a monitoring mode is emitted through an output associated with a predetermined counter position whereby a second reference value is loaded into the first partial shift register (2) and a third reference value into the second shift register (3) and that the output of the second shift register (3) is connected to a switching member (20) conveying the arriving data stream by a logical element (15, 16) whereby a monitoring signal appears at the output of the logical element (16).

3. Circuit arrangement in accordance with Claim 2 or 3, characterised in that, the switching member (20) conveying the arriving data stream contains a data modifying circuit which comprises a number of EXCLUSIVE-OR elements (17, 18) corresponding to the number of data items that are to be modified and whose inputs are connected to outputs of adjacent storage cells (D, Q; Q, Q1) of the shift register (1, 2) and that the outputs of the EXCLUSIVE-OR elements (17, 18) are connected to outputs of the control circuit (8) by AND elements (20a, 20b) whereby control signals (ABF1, ABF2) occur on the outputs of the control circuit (8) at the time point of the data items that are to be modified.

