

ABSTRACT

The present disclosure relates to a semiconductor device, and a semiconductor device according to an embodiment includes a substrate that includes a first well region having a first conductivity type and a second well region having a second conductivity type, a first lower pattern positioned in the first well region, a second lower pattern positioned in the second well region, a first channel pattern positioned on the first lower pattern, a second channel pattern positioned on the second lower pattern, a gate structure that surrounds the first channel pattern and the second channel pattern, a first source/drain pattern positioned on opposite sides of the first channel pattern, a first well tap pattern positioned on opposite sides of the second channel pattern, and a first barrier pattern positioned between the first source/drain pattern and the first lower pattern.

FIG. 3