ABSTRACT

A method for making novel elevated bond-pad structures with sidewall spacers is achieved. The elevated bond-pad structures increase the space between the chip and a substrate during flip-chip bonding. The increased spacing results in better under-filling and reduces alpha particle soft errors in the chip. The sidewall spacers restrict the wetting surface for the PbSn solder bumps to the top surface of the bond pads. This results in smaller solder bumps and allows for closer spacings of the array of bonding pads for higher density integrated circuits.

Figure 7