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COMPLETE SPECIFICATION.

Modular Integrated Electronics Radar.

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to radar involving solid-state microwave modules, and more particularly to a modular electronic radar having a multi-element phased array antenna.

While this invention is immediately advantageous in connection with construction and operation of airborne radar, it has application to other radar systems such as those used for ground mapping, search and detection, fire control, tracking, and navigation and may be programmed to operate in any one of the above modes or in several of such modes on a time-sharing basis.

Airborne radar systems have been faced with the problems of minimizing the weight and increasing the reliability. Other problems involve the generation of high power microwave energy and the requirements for involved signal process and for computing circuitry.

It is well known that the major problems in radar have been concerned with auxiliary equipment such as rotary joints, servo motors for the antennas, and the like. These restrictions on reliability exist in the most modern of all transistorized radars produced for airborne service. Further, the use of

magnetrons for transmitting, klystrons for local oscillator service, and use of high power transmit-receive (TR) protection devices, all have been found to restrict the reliability of the system.

It is an object of the present invention to provide a radar in which solid-state circuitry is so constructed and arranged as to be capable of overcoming the major obstacle heretofore encountered in the development of solid-state radar, namely, the generation of high power microwave energy. This problem is overcome by use of solid-state functional electronic blocks or modules, so constructed as to operate as a modular antenna array which may be responsive to beam steering control and which may be operated at an adequate power level at the X-band (8.5—10.5 giga hertz) frequencies of, for example, 9 Gc (9×10^9 cycles per second).

In a radar having an antenna formed by a multiplicity of modules each having radiation structure and forming substantially a planar radiation array, each module including an RF unit, a phase shift unit, and a control network, the present invention, provides a method which comprises:—

(a) applying a pulse of an RF carrier coincident in time and in phase to each of said modules,

(b) simultaneously applying an in-phase impulse of a phase control carrier to each of said modules,

(c) shifting the phase of the phase control carrier pulse in each said module by phase angles dependent upon the position of each module in said array and in de-

pendence upon a predetermined beam angle,

(d) mixing each phase shifted phase control carrier pulse with the RF carrier pulse,

(e) amplifying one of the modulation products from the combined phase control carrier pulse and the RF carrier pulse for excitation of said antenna,

(f) sensing electromagnetic energy reflected to said antenna to produce a received signal in each module,

(g) shifting said received signal in each module by a phase angle related to the shift in said phase control carrier pulse, and

(h) combining all of the phase shifted received signals from said modules to produce an output signal.

In a radar having an antenna formed by a multiplicity of modules each having radiation structure and forming substantially a planar radiation array, each module including an RF unit, a phase shift unit, and a control network, the present invention provides a method which also comprises:

(a) applying RF carrier pulses and power to said modules,

(b) shifting the phase angle of the RF carrier pulses in each of said modules with patterned gradation across said array related to the position of a given module in said array and related to a predetermined antenna beam angle,

(c) amplifying the phase shifted RF carrier pulses to produce RF carrier pulses of enhanced power,

(d) multiplying the frequency of the amplified RF carrier pulses, and

(e) converting the resultant signals into electromagnetic radiation beamed from said array in dependence upon said patterned gradation.

In a radar having an antenna formed by a multiplicity of modules each having radiation structure and forming substantially a planar radiation array, each module including an RF unit, a phase shift unit, and a control network, the present invention provides a method which also comprises:

(a) controlling the phase of an RF signal having a relatively low frequency in accordance with the position of an element in the array,

(b) amplifying the controlled phase RF signal to enhance the power to a level in excess of the power to be applied to the radiation element,

(c) multiplying the amplified RF signal to produce a signal in the desired frequency band, and

(d) exciting the element with the multiplied RF signal.

A radar having an antenna formed by a multiplicity of modules forming substantially a planar radiation array, the present invention also provides that each of the modules comprises:

(a) a radiation structure,

(b) a solid state mixer and power amplifier connected in series between an RF input terminal and the radiation structure for pulsed excitation of the radiation structure,

(c) a variable phase shift circuit connected between a phase control carrier terminal and the mixer for controlling the phase of the pulse applied to the radiation structure,

(d) a frequency multiplier circuit for increasing the frequency of the signal from the RF input terminal to the radiation structure, and

(e) a receiving channel leading from said radiation structure and through the phase shift circuit to an output terminal.

The present invention also provides a radar having an antenna formed by a multiplicity of modules, each having radiation structure and forming substantially a planar radiation array comprising:

(a) means to provide separate first signals of like frequency and phase for each of said modules,

(b) means within each of said modules to multiply the frequency of said first signal thereby to provide a second high frequency signal within said module, and

(c) means to impose a separately-controllable phase shift upon each of said first signals prior to frequency multiplication thereof.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 diagrammatically illustrates the operation of an aircraft, its antenna array, and the functional electronic block employed to make up the array;

Figure 2 illustrates one form of a solid-state antenna module;

Figure 3 is a block diagram of the terrain-following radar of Figure 1;

Figure 4 is a block diagram of the electronics in each module;

Figure 5 is a top view of a solid-state mixer circuit of Figure 4 comprising a surface-oriented diode, a strip transmission line, and a coupler;

Figure 6 is a sectional view taken along line 6—6 of Figure 5 illustrating a planar alloy, surface-oriented diode;

Figure 7 is a modified form of surface-oriented diode in which diffusion techniques are employed;

Figure 8 is a top view of the surface-oriented diode;

Figure 9 illustrates preliminary steps in forming a diode similar to that of Figure 7;

Figure 10 illustrates further processing steps in forming a diode similar to that of Figure 7;

Figure 11 is a top view of the diode structure of Figure 10;

Figure 12 is a modified mixer construction employing a surface-oriented diode wafer and ceramic substrate;

Figure 13 is a lumped constant diagram of the multiplier circuit of Figure 4;

Figure 14 is a top view of an integrated circuit embodiment of the multiplier of Figure 13;

Figure 15 is a sectional view taken along lines 15-15 of Figure 14;

Figure 16 is an enlarged view of the fabrication sequence of the diode of Figure 14 in planar form;

Figure 17 is a sectional view of a multiplier in which a mesa diode is employed;

Figure 18 is a reactance vs. frequency diagram for the multiplier circuit;

Figure 19 illustrates a phase shift delay strip-line panel;

Figure 20 is a sectional view of the integrated circuit of one unit of Figure 19 taken along lines 20-20;

Figure 21 illustrates a video amplifier construction for the IF preamplifier of Figure 4;

Figure 22 is a top view of antenna 12 illustrating beam-scanning;

Figure 23 is a schematic diagram illustrating distribution of reference voltages to the antenna modules;

Figure 24 illustrates generation of reference voltages for the antenna modules; and

Figure 25 is a time plot of the sequence of operation of the radar of Figure 4.

The invention will be described as it is employed in a terrain-following radar. In this system, an aircraft 10 has an antenna unit 12 mounted in the nose 13. Antenna unit 12 is comprised of a multiplicity of functional electronic blocks or modules, such as the block 14. In the embodiment illustrated in Figure 1, 448 such blocks make up an antenna array of octagonal shape. The face of each block is of the order of one inch (1") square. Block 14 is adapted to be plugged into a suitable frame in the antenna unit 12 to transmit and receive electromagnetic energy by way of slot 15.

The video information made available by the radar is then processed to provide terrain-following capabilities. For example, in accordance with one mode of operation employed in a system known as the template system, a pre-master trigger is supplied to the template generator concurrently with each transmitted pulse from the antenna unit 12 to initiate a synthetic echo. This echo or template trigger occurs at a time range that is based upon the desired clearance altitude, the characteristics of the air frame, and the scan position. The range of the template trigger changes with the scan angle.

The scan angle is varied by adjusting the relative phase relationships between the microwave energy applied to each of the modules in the antenna unit 12 during one vertical scan. The scan angle defines the template shape such as illustrated in Figure 1 by the outline 16. The video return or received signals are compared with the synthetic echoes to obtain proportional command signals. The video return signal received before the synthetic echo signal is employed to generate climb commands. Similarly, the video return signal received after the synthetic echo generates dive commands.

The modules of antenna unit 12 are of identical construction and may be of the character illustrated in Figures 1 and 2, where a planar face member 20 is provided with a slot 15 leading to microwave circuits which are excited by pulses of an RF carrier of X-band frequency.

Antenna module 14 includes its own power generation circuit and receiver pre-amplifier circuit and in addition has its own phase shift circuit for beam steering.

The size of the module is determined or limited by the allowable spacing between radiating elements for avoidance of spurious grating lobes.

SYSTEM BLOCK DIAGRAM

As shown in Figure 3, module 14 includes an RF unit 30, a phase shift unit 31, and a control network 32. The phase shift unit receives low-power RF carrier pulses by way of a channel 33 and delivers output signals of IF frequency by way of channel 34. A beam steering or phase control voltage is applied to the control network 32 by way of channel 35. While only one module 14 has been shown in Figure 3, it is to be understood that the 448 blocks illustrated in the antenna unit 12 of Figure 1 will similarly be excited and controlled from a manifold 40.

A source 41 supplies a pulsed RF carrier at 2.125 Gc to manifold 40 under the control of a pulse generator 44. An oscillator 42 supplies a pulsed phase control carrier at 125 Mc to the manifold 40. As will hereinafter be explained, the phase control carrier is employed for introducing a selected phase shift into the RF pulse from source 41. A local oscillator 43 applies a continuous low level voltage to manifold 40 at a frequency of 8.5 Gc.

Output signals at an IF frequency appear on channel 34 and are applied from module 14 to manifold 40 for processing. As indicated, the IF signals from modules in the upper quarter of the antenna unit 12 are summed and appear on output channel 45. The sum of the IF output signals from the upper centre quarter of the antenna unit 12

appears on channel 46. The sum of the IF output signals from the lower centre quarter of the antenna unit 12 appears on channel 47, and corresponding signals from the lower quarter of antenna unit 12 appear on output channel 48.

Channels 45 and 47 are connected to the inputs of a 3 db hybrid coupler 50. The signals on channels 46 and 48 are applied to the inputs of a coupler 51. One output from coupler 50 is applied to a coupler 52 by way of a 45° phase delay unit 53. The second input to coupler 52 is supplied by one output of coupler 51. In a similar manner, a fourth coupler 54 is supplied by way of a phase delay unit 55 and by coupler 50. The output signals from couplers 52 and 54 are applied to IF amplifiers 56 and 57, respectively, which in turn feed pulse compression filters 58 and 59. Detectors 60 are driven by output signals from filters 58 and 59 and in turn drive a monopulse resolution improvement processor and video amplifier 61. A signal recognition circuit 62 excited by unit 61 drives a command computer 63, one output of which may be applied by way of a converter 64 to an autopilot 65.

An automatic gain control (AGC) 66 excited by the output of unit 61, controls IF amplifiers 56 and 57. A sensitivity time control (STC) unit 67 also feeds IF amplifiers 56 and 57 under the control of a timer synchronizer 68. Synchronizer 68 also feeds the command computer, as do command input function generators 69—73. Generator 69 is a scan computer indicating the direction of the antenna beam. If an objective is present, then the system generates a control signal for autopilot 65. Generator 70 provides a signal representative of velocity of the aircraft. Generator 71 generates a signal representative of the actual flight vector. Generator 72 is a ride control generator, and determines whether a rough or smooth course is followed, i.e., how abruptly the aircraft will change attitude when a target or obstacle is sensed. Generator 73 generates a signal representative of the aircraft pitch angle.

In the light of the foregoing description, it will be recognized that exacting requirements are placed upon the elements to be included in module 14. In order to provide antenna power at the level necessary, solid-state circuits are employed with circuit configurations such that the necessary power may be supplied to the antenna and the desired versatility and control there are available within the capabilities of solid-state semiconductor networks.

ANTENNA MODULE CIRCUIT

Figure 4 is a lumped constant representation of integrated circuits for: (a) receiving

modulated RF carrier pulses at a relatively low-power level from channel 33; (b) receiving phase control carrier pulses on a channel 83; (c) shifting the phase of the phase control carrier in the phase shift unit 31; (d) modulating the RF pulses with the phase shifted pulses in a mixer 85; (e) amplifying one of the modulation products in the power amplifier 30; (f) stepping up the frequency of the high power signal in the frequency multiplier 86; (g) applying the final output pulses to an antenna 87; (h) detecting return signals to the antenna 87; (i) mixing the same in a mixer 88 at the input of a preamplifier 89; and (j) passing the detected signals from amplifier 89 through the phase shift unit 31 for delivery to an output channel 34.

For the purpose of the present example, the operation will be such that the RF pulses applied to channel 33 will be at a frequency of 2.125 Gc, ± 0.625 Mc, the swing of 1.25 Mc being from low frequency to high frequency by pulse generator control of the oscillator 41 as shown in Figure 3. The phase control carrier applied to terminal 83 will be at 125 Mc. The signal applied to the antenna 87 will be 9 Gc and the output signal on channel 34 will be at 500 Mc. The module delivers one watt peak power to the antenna 87 at 9 Gc.

The modulated RF carrier pulses applied to the channel 33 pass through a tuned filter 100 at the input of the mixer 85. A second tuned filter 101 is located in the output channel leading from the phase shift unit 31 and is tuned to 125 Mc for modulating the 2.125 Mc carrier pulse. The output circuit 102 is then tuned to the upper side band or 2.250 Gc for driving the power amplifier 30. The phase shifting unit 31 is employed to control the phase of the carrier at the output tuned circuit 102.

PHASE SHIFTING

BY LINE LENGTH SWITCHING

Beam scanning is provided for the antenna made up of a plurality of modules 14. As shown in Figure 4, beam scanning is produced by switching discrete lengths of transmission line into the antenna feed system and more particularly into the channel through which the 125 Mc phase control carrier is transmitted. This is a step-type phase shifter. The size of the smallest step is important in determining the complexity of the control circuit. In the unit 31, five transmission lines are employed and are of such length as to provide phase delay units 111—115 of 11¼°, 22½°, 45°, 90°, and 180° delays, respectively, at a frequency of 500 Mc. The 125 Mc signal applied to terminal 83 will undergo delays one-fourth of the amounts noted.

The phase shifter and switching unit 31

includes diodes 120 and 121 forming an input switch. The common juncture between diodes 120 and 121 is connected to diode switches 122 and 123. Delay line 111 is connected to diode 123 and thence, by way of diode 124 and condenser 125, to the input channel 126 leading to the second stage of the phase shifter 31. The diode 122 is connected by way of condenser 127 to channel 126. The switches 122, 123, and 124 are selectively biased under the control of a bistable multivibrator 128. A second multivibrator 129 controls transmission through, or the bypass channel for, the second delay line 112. Multivibrators 130, 131, and 132 similarly control inclusion or deletion of lines 113, 114, and 115, respectively, from the transmission channel for the 125 Mc phase control carrier. A sixth multivibrator 133 is connected to the output of multivibrator 132 and in turn feeds a TR switch comprised of diodes 137 and 138.

The switch control line 140 leading to the multivibrator 128 is supplied from a clock input channel 141 at 1 Mc by way of an AND gate 142. The second terminal of the AND gate is fed by voltage comparator unit 143. The line 144 of multivibrator 128 is connected by way of condenser 145 to the input line 146 of multivibrator 129. Similarly, condensers 147-149 connect multivibrators 129-133 in a binary counter configuration. From zero phase delay, the first clock pulse actuates multivibrator switch unit 128 to include line 111 in the 125 Mc circuit. The second clock pulse actuates units 128 and 129 to remove line 111 and to include line 112. The third pulse actuates unit 128 to include line 111 with line 112. The fourth pulse actuates units 128, 129, and 130 to remove lines 111 and 112 and to include line 113. Thus, a digital progression is employed in increasing the delay in the delay line unit.

The multivibrator 128 is coupled by way of lines 151 and 152 to a digital-to-analog converter 153. Similarly, all of the other multivibrators are coupled to the digital-to-analog converter so that the state of the switching networks is indicated by an analog signal on the output line 154. Switch unit 133, while introducing no delay, applies current to converter 153 proportional to 360° phase delay so that the line switching sequence may continue through two cycles or 720°. The output signal from converter 153 is applied to the second input of the voltage comparator 143.

In operation, a reference voltage representative of the desired phase delay for module 14 is applied to the input terminal 35. So long as the reference voltage exceeds the output from the converter 153, the output from the comparator 143 enables the AND gate 142. With the AND gate 142

conductive, the clock pulses from terminal 141 successively shift conduction between the various bistable multivibrators. When the output of the converter 153 equals the reference voltage on channel 35, the AND gate 142 discontinues transmission of the clock pulses and the desired delay is then fixed in the phase shift unit 31. Thereafter, the simultaneous application of the RF carrier pulse and the phase control carrier pulse to terminals 33 and 83, respectively, will produce a pulse of 2.25 Gc at the output of the tuned circuit 102 in the mixer 85. The phase of the 2.250 Gc signal at circuit 102 is equal to the phase delay in the unit 31.

The signal from mixer 85 is then applied to the power amplifier 30 for delivery of about two watts peak power at 2.25 Gc to the input of the frequency multiplier 86. The multiplier 86 consists of resonant circuits in which a diode 160 is the active element. The multiplier is a quadrupler for delivery to the output channel 161 of a pulse whose frequency is 9 Gc at a peak power level of about one watt. The latter pulse is applied by way of a TR switch diode 162 to the antenna 87 for radiation at the phase set by the phase delay unit 31.

Immediately after pulse transmission from the antenna, the control multivibrator 163 for the TR switch 162, 164 changes state so that return signals detected by the antenna 87 pass through TR switch diode 164 to the input to a mixer 88. The mixer 88 is supplied with an 8.5 Gc local oscillator signal on channel 165. The lower side band modulation product at 500 Mc is applied to the IF preamplifier 89. The latter signal then passes through the switch diode 138 and the phase shift unit 31 where the signal undergoes a delay of four times the delay of the phase control carrier. This is with the same delay unit setting as employed during the transmit operation. The delay IF signal then passes through the output switch diode 121 to the output channel 34 leading to the manifold. While not shown, control units for TR switch 120, 121 and TR switch 137, 138 will provide bias voltages therefor in the same manner as the bias is supplied TR switch 162, 164.

More particularly, it will be recalled that the phase control carrier applied to terminal 83 was at a frequency of 125 Mc, and that it passed through the phase shift unit 31 to control the phase of the IF pulse applied to the antenna 87. Since the multiplier 86 quadruples the frequency, the phase shift introduced by the unit 31 is also quadrupled in the antenna drive signal as it appears on channel 161. Thus, with the output of the IF preamplifier 89 at 500 Mc, the output signal on channel 34 will have exactly the same phase shift as introduced into the an-

tenna drive pulse. Thus, the same phase shift unit is used for both the transmit and the receive cycle and the beam direction is the same for receiving as for transmitting.

5 With power amplifier 30 present, module 14 includes its own power generation means and thus operates on low level signals from the manifold. The circuit 30 raises the power level by about 20 db in the preamplifier section 30a, about 6 db in the driver 10 30b, and about 4 db in the output section 30c. By way of example, the power applied to the input of the preamplifier would be about 2 milliwatts (mw) peak or 0.2 mw average power. The signal at the input to 15 the driver 30b would be at about 200 mw peak or 20 mw average. The power applied to the output stage would be about 800 mw peak or 80 mw average. The power output from the output stage would be about 20 2 watts peak or 0.2 watts average power. In accordance with the construction hereinafter to be described, the multiplier would operate to increase the frequency from 2.25 25 Gc to 9 Gc with an insertion loss of 3db to provide one watt peak power to the antenna 87. Thus, the power generation chain consists of 3 or 4 amplifier stages at 30 2.25 Gc followed by a quadrupling multiplier with an output at 9 Gc.

MIXER

In the system illustrated in Figure 4, as in other microwave systems where a high-frequency, low-level return signal is employed, the quality of the receiver largely 35 determines the other system parameters. For operation at frequencies transmitted by antenna element 87, the noise level of the mixer 88 presents the principal problem and the mixer comprises a critical and principal 40 component of the receiver portion of Figure 4.

Mixer 88 converts the received signal to a lower frequency preferably with a minimum of added noise. To optimize the noise level for the receiver, both the signal-to-noise ratio of the mixer and the conversion loss in the mixer must be as low as possible. The detected signal from diode 164 and a 50 local oscillator output signal on line 165 of Figure 4 are applied to a semiconductor junction and the difference as IF output signal is extracted.

For operation at frequencies in the X-band (i.e. 8.5—10.5 giga hertz), the mixers 55 illustrated in Figures 5—12 may be employed. Operation thereof is characterized by low loss, employing power splitting couplers of integrated circuit form.

60 More particularly, as shown in Figure 5, a semiconductor wafer 210 is provided with a signal input strip 211 and a local oscillator input strip 212. Strips 211 and 212 are metalized regions overlaying a high resisti-

vity semiconductor wafer. The metalized regions 211 and 212 lead to the input portions of a hybrid coupler 213. The coupler 213 is provided with parallel sections 214 and 215 which are about one-quarter wavelength long and are of a width substantially greater than the width of the strips 211 and 212. Two shunt strips 216 and 217 are spaced approximately one-quarter wavelength apart and extend between sections 214 and 215. Output lines 218 and 219 75 extend from the coupler 213.

A pair of quarter-wave transformer sections 220 and 221 extend from the output strips 218 and 219, respectively, and make contact with terminals of surface-oriented diodes 222 and 223, respectively. Output conductors 224 and 225 lead from the other terminals of diodes 222 and 223 to output capacitors 226 and 227 to provide an output signal at output terminals 228 and 229. 85

With strip-line transmission lines overlaying the semiconductor wafer 210 and with surface-oriented diodes of a construction hereinafter described, a signal in the X-band may be converted to IF with about a 5 db loss. For example, a 9 Gc signal may be applied to strip 211. A local oscillator signal at 8.5 Gc may be applied to the input strip 212. As a result, an IF signal of 500 95 Mc is produced at terminals 228 and 229.

The surface-oriented diode 222 is illustrated in one form in Figure 6. The wafer 210, of intrinsic silicon, is provided with a ground plane conductive layer 230. The intrinsic silicon forms a high resistivity zone 100 above the ground plane layer 230. An N-type alloyed region 231 and a P-type alloyed region 232 are formed in the surface of the wafer 210 opposite the ground plane layer 230. A silicon dioxide insulating layer 233 105 is formed over the upper surface of wafer 210 to cover the surface emergence of the junctions forming the boundaries between the P-type and N-type alloyed sections and the intrinsic wafer 210. An N-type metal 110 alloy strip 220 is then formed on the surface of the wafer 210 so as to make electrical contact with the N-type region 231. A P-type metal alloy strip 224 is formed on the surface to make electrical contact with the 115 region 232. The P-type and N-type metal alloy strips 220 and 224 are evaporated onto the surface through holes in oxide masks defined by photolithographic techniques. The metal alloy strips are then alloyed into the 120 silicon to produce the N+ and P+ regions between the strips and the N-type and P-type regions 231 and 232. An intrinsic region 234 is disposed between the N and P regions, the boundary junctions of which 125 are shown in dotted outline.

Such fabrication of the surface-oriented mixer diode is in a form compatible with the integrated circuit construction. The

diode is a substantial improvement over conventional microwave mixer elements. Previous mixer diodes have been of the point contact variety in order to maintain low junction capacitance. The present construction has achieved junction capacitances of 0.05 pico farads (pf) or less. When biased by rectification of the local oscillator signal to obtain the best noise figure, the shunt resistance of the junction is approximately 400 ohms. In ordinary mixer diode configuration, this value of resistance is transformed to an input impedance of about 50 to 100 ohms by the package inductance and the junction capacitance. In the present case, the junction diameter of the diode is approximately 0.1 mil (0.0001 inch). Production of a semiconductor junction of this size, as above noted, employs intrinsic silicon having side-by-side alloy zones to form confronting edge junctions that will give the surface diode effect.

The material required for the integrated circuit preferably will provide a suitable substrate for microwave strip transmission lines and for forming the mixer semiconductor junctions. Intrinsic silicon and high resistivity gallium arsenide may be employed for mixer diodes, whereas germanium has characteristics which are not suitable for both the microwave strip transmission line and the diode construction. Where extremely low loss transmission lines are required, low loss dielectrics with deposited silver conductors are employed. Yttrium-iron-garnet (yig) substrates may also be employed for this purpose.

Figure 7 illustrates a modified form of surface-oriented diode wherein side-by-side diffusions of opposite-conductivity type impurities are formed on the upper surface of an intrinsic silicon wafer 240. The N-type diffusion zone 214a and the P-type diffusion zone 242a are characterized by an edge junction that will give the surface diode effect. The zones 241a and 242a are formed partially in N+ and P+ diffusion zones 241 and 242, respectively, which in turn are formed in an insulated island of intrinsic silicon about 1 mil wide and 5 mils long formed in the wafer by an insulating layer 243 of silicon dioxide.

The spacing between the edges of the diffused N+ and P+ zones 241 and 242 is about 0.3 mil in zone 247. However, the zone 248 between the confronting junctions of the N and P zones 241a and 242a is about 0.1 mil wide. The capacitance of the junction is defined by the effective junction area of shallow diffusions and the reverse breakdown by the shallow diffused spacing and intrinsic or I-layer concentration. Conductivity modulation under forward current conditions is minimized by reason of the effective increase in injection area

of the anode of the deep P+ diffusion. The problem is in defining the I-layer between the diffusion fronts so that a sufficient current density can be obtained at reasonable current levels. For currents of 20 milliamps, about a 4 square mil area will give a current density of 200 amps per square centimetre required for conductivity modulation. An insulating layer 244 covers the surface of the wafer except for metalized contact zones 245 and 246.

Surface-oriented diodes of the type illustrated in Figures 6 and 7 may be employed in the mixer of Figure 5. Where additional current-carrying capacity is required of surface-oriented diodes, as in the transmit-receive switches employed in Figure 4, the construction such as shown in Figure 8 may be employed.

In Figure 8, the transmission lines 220 and 224 are shown contacting the diffused zones 241 and 242, respectively. The diffused zone 241 has three fingers. The zone 242 has two fingers with the fingers being enmeshed or interdigitated to provide a junction of high current-carrying capability. Such a construction exhibits low junction capacitance under moderate reversed-bias conditions and low loss.

Intrinsic silicon as the substrate material for the diodes provides insulation for any number of components deposited upon it and also provides a low loss structure. The structure is readily adaptable to receive strip transmission lines deposited directly onto the silicon. In accordance with one mode of fabrication, a ground plane conductor is evaporated onto the bottom of an intrinsic silicon substrate of approximately 5 mils thickness. Silicon dioxide on the top is etched to expose the silicon where transmission lines are required. Gold is then evaporated over the entire surface and selectively removed to leave gold over the exposed regions of the silicon. Preferably, in order to maintain the propagation properties of the lines, the alloying of gold with silicon will be avoided, as by the forming of a thin layer, a few microns thick, of a material such as molybdenum between the gold strips and the silicon.

As an alternative mode of fabrication, a hot substrate evaporation of gold onto the intrinsic silicon is carried out. The gold is then etched away to leave the transmission lines where required. At microwave frequencies, the degradation of leakage current due to the introduction of the gold into the silicon is of little consequence. In the same manner, aluminium strip transmission lines may be formed on gallium arsenide to form the transmission line pattern on a given substrate. Thus, the mixer of Figure 2 is a flat, integrated circuit package. The integrated circuit may be part of more complex circuits

formed on the same or interconnected substrates.

Referring again to Figure 7, a diffused, surface-oriented diode is shown with insulation isolation. One procedure for forming this structure is shown in Figures 9—11. The structure illustrated in Figures 9—11 is similar to the structure illustrated in Figure 7, and corresponding parts will therefore be designated by corresponding reference numerals. However, the structure of Figures 9—11 is illustrated as round, while the structure of Figure 7 is rectangular. The surface of a single crystal, high-resistivity substrate of N-type material is etched on the surface to form a mesa 240a on the top surface. The oxide layer 243 is then grown over the upper surface of the etched wafer and over the mesa 240a to form an insulating layer over the entire etched surface. The material forming the bulk substrate 210 of the structure in Figure 7 is then deposited or grown over the top of the slice 240 to completely cover the insulation layer 243 and to surround the insulation covered mesa. After the bulk material 210 is grown onto the top of the wafer, the top (in Figure 9) of the bulk material 210 is lapped smooth for receiving the ground plane conducting layer 230 shown in Figure 7.

The substrate 240 is then lapped so that all of the original wafer is removed except for the mesa which is then the island 240a located in a well or depression surrounded by the isolation layer of silicon oxide 243 as shown in Figure 10. Thereafter as shown in Figure 11, through a photomasking technique, N+ and P+ diffusions are made to form the zones 241 and 242 of opposite-conductivity types in the island 240a. Inside the island there is then high enough impurity concentration for good low resistivity ohmic contact. The low resistivity (high concentration) diffusions have a very narrow intrinsic zone between them, of the order of 0.3 mil wide. Into this area of original material, there are made two very shallow diffusions 214a and 242a of N and P-type materials, respectively. The diffusions are very shallow (3 lines or 3×0.016 mil) with high concentrations. The junction between the N and P shallow diffusion zones 241a and 242a is not or need not be accurately positioned as long as it is within the 0.3 mil strip. The junction between the two zones is 1 mil wide and 3 lines deep or an area of $1 \times 3 \times 0.016$ mil = 0.048 sq. mil. This results in a very low capacitance junction suitable for use in the mixer of Figure 5. Contacts 245 and 246 are readily applied to the two N+ and P+ regions of Figures 10 and 11 to be used for bonding or pressure contacts alloyed in.

Where the diode is to be employed in the mixer application, the separation 248, Figure

7, between the junctions will be reduced to zero. The boundaries of the two zones will thus be contiguous. Surface-oriented diodes for use in switching applications will be constructed with separation between the two zones and for high current capability, will be interdigitated as shown in Figure 8.

In Figure 7, transmission lines 245 and 246 extend along the top of the insulating layer 244 from contact with the zones 241 and 242. Preferably, the transmission line leading to and from the surface-oriented diode, except for the insulation over the junctions as shown in Figure 7, will be formed directly on the surface of the semiconductor material 210. Preferably, ground plane conductor 230 and the low resistance conductive strips 245 and 246 are gold and overlay an extremely thin film of a metal such as molybdenum, as above noted, or of vanadium, platinum, nickel or tungsten evaporated to a thickness of a few microns to form an underlayer for each strip. The underlayer having a high eutectic temperature will prevent the formation of lossy zones that would otherwise be present where gold strips to be formed directly onto the silicon surface and then subjected to treatment at temperatures wherein the silicon would become intermixed with the gold at the boundary thereof. Such zones are avoided by the use of the thin film 249. The ground plane layer 230 is shown as having been formed over a film 249a on the bottom surface of the structure as shown in Figure 7 where the film 249a would be of materials the same as film 249.

Thus, for switching use, the diode junctions are spaced apart to form a PIN diode junction. For mixer use, the confronting portions of the junction are contiguous or overlap to form a PN diode junction. In the latter case, the boundary of the last diffused zone would define the diode junction.

In Figures 6—11, surface-oriented diodes are formed in a semiconductor substrate and thus involve a single basic building material. In Figure 12, a modified form of mixer construction has been illustrated. In this embodiment, a relatively thick high dielectric constant ceramic layer 251 has a ground plane conductive layer 252 on the bottom face thereof with a thin high eutectic metallic layer 252a therebetween. The strip-line conductors 253 and 254 are formed on the upper face of the ceramic substrate 251. A surface-oriented diode 255 having diffused P and N-type zones 256 and 257 formed therein is then employed in a sandwich construction to form a diode which corresponds with the diode 222 of Figure 5. The diode 255 is formed in a thin wafer or chip of semiconductor material and then placed face down onto the ends of the strip-like conductors 253 and 254. An isolated insulation

130

layer 259 is then formed over the top of the ceramic substrate 251 to encompass the diode 255. A glass evaporate layer 258 is then deposited on top of the insulated layer 259. A high eutectic metal layer 260 with a ground plane surface conductive layer 262 is then formed on top of the layer 258. A conductor serves to connect the ground plane layers 252 and 262 together for forming a shielded sandwich construction for the mixer transmission line elements and the surface-oriented diode.

FREQUENCY MULTIPLIER

The frequency multiplier 86 of Figure 4 has been further illustrated in a lumped constant equivalent form in Figure 13. The L matching section includes a series inductance 310 and a shunt capacitance 311. A low pass filter comprised of series inductances 312 and 313 and shunt capacitance 314 provides a low pass filter tuned to 2.25 Gc. The resonant circuit which includes the active element is comprised of series inductances 315 and 316. A shunt capacitance 317 is connected to the juncture between inductances 313 and 315. A series resonant shunt circuit comprised of inductance 318 and capacitance 319 is connected to the juncture between inductances 315 and 316. A shunt circuit comprised of an inductance 320 and a diode 321 is connected to the juncture between inductance 316 and the series inductance 322 forming a part of the output band pass filter. The band pass filter includes series inductance 322, capacitance 323, capacitance 324, and series inductance 325. Shunt capacitance 326 is connected to the juncture between capacitances 323 and 324. The output L matching section includes series inductance 327 and a shunt capacitance 328.

The formation of the multiplier in one integrated circuit configuration is shown in Figures 14 and 15. Prior art systems generally are limited as to power level at frequencies such as encountered in the X-band because of the small geometry necessary for operation. For example, over 25 watts power output is available from a single transistor at frequencies as high as 100 Mc. For amplifiers utilizing one transistor per stage at 1000 Mc, about 200 milliwatts are available and at 3000 Mc, this is reduced to about 10 milliwatts. The large power capabilities at lower frequencies and efficient frequency multiplication are combined in the system shown in Figures 14 and 15 to obtain the necessary power at high frequencies. By this means, peak power output capability of integrated microwave sources of about 1 watt can be obtained at frequencies well above 8 Gc.

The multiplier shown in Figures 14 and 15 employs a varactor diode 321 operating

as a quadrupler with idlers at second and third harmonics. More particularly, the tuned circuit 318 and 319 may be considered to be resonant at the second harmonic and the tuned circuit 320 and 321 at the third harmonic. Because of integrated circuit construction, rather than lumped constant construction, there is contribution to the several resonance conditions from most or all of the elements in the unit since isolation of any one element is not possible as in lumped constant circuit construction. Therefore the description as to resonant circuits is in terms of result with a construction shown in Figure 14. The circuit will change the frequency from an input frequency of 2.25 Gc to an output frequency of 9 Gc.

As shown in Figures 14 and 15, the varactor diode and the strip-line transmission circuits forming inductance and capacitance are formed on a semiconductor substrate. The substrate 330 has about one half of its area covered by a highly conductive surface layer 329. The layer 329 is then covered by a thin dielectric layer 339 so that layer 329 serves as a common plate for all but two condensers in the multiplier.

The input L section is formed by the strip transmission line 310 which extends over the thick dielectric portion of the substrate 330 to the plate 311 of the input capacitor. The capacitor 311 overlays the relatively thin dielectric layer 339 to form a condenser with the common conductive layer 329. The loop 312 forms an inductance over the thick dielectric layer and leads to a capacitor plate 314 over the thin dielectric layer. Similarly the loop 313 leads to the capacitor plate 317. The transmission line filter system will thus be characterized by long thin transmission lines over thick dielectric sections to provide primarily inductance characteristics. Wide transmission line sections overlaying thin high dielectric layers form zones in the transmission line system primarily capacitive in nature. The loop 315 extends from plate 317 over the thick dielectric to the juncture with a loop 318 which leads to a capacitor plate 319. Loop 315 also leads to one terminal of the varactor diode 321. A strip extending from the juncture 320 and loop 322 then leads to a capacitor plate 323. The capacitor plate 323 is positioned on top of a conductive layer 340 which overlays one-half of the condenser plate 326. Condenser plate 324 similarly overlays the plate 326. The transmission line loop 325 then extends to the output capacitance plate 328 with the matching inductance 327 extending from the plate 328. The plate 326 is capacitively coupled to the capacitor plates 323 and 324 and to the high conductive layer 329.

For frequencies within the range of from 0.5 to 5 Gc, input and output impedance will be on the order of from 10 to 50 ohms

Capacitance values will be within the range of from 5 to 75 pico farads (pf) (10^{-12} farads) and inductances between 0.5 and 10 nanohenries (nh) (10^{-9} henries).

5 Since relatively high Q capacitances are necessary for operation of the multiplier circuit, an extremely thin, high dielectric constant layer 339 is employed. The inductances have low loss and high effective inductance per unit length. Thus, in the planar construction of Figures 14 and 15 large spacing between thin conductive loops on the upper surface of the slice 330 and the ground plane conductor form inductances. 10 In contrast, the wide conductive layers 339 and 340 over a thin high dielectric layer form capacitances. Preferably the substrate 330 will have a dielectric constant of the order of from 4 to 12 and a thickness of from 0.005 to 0.010 inches. The layers 339 and 340 will have a dielectric constant of about 40 to 50 and a thickness of 0.0001 inch.

25 The filters at the input and output of the multiplier form traps to prevent power flow from the multiplier other than at the desired frequency. At the same time, the dissipation of power in the varactor is held at a minimum while maintaining the necessary band width of the multiplier. A band width (about 8.5—9.6 Gc) is required due to both the characteristics inherent in the operation of the non-linear reactance or diode 321, and the undesired variations in temperature of the semiconductor junction capacitance. 30 The multiplier band width must be sufficient to allow buildup of voltage amplitude across the diode junction, and thus develop bias voltage to bring the multiplier into proper operating range.

40 The requirements for both the capacitors and inductors thus may be fulfilled on the common substrate or slice 330. Diode fabrication techniques indicated in Figure 16 may be followed.

45 In step (a), N-type material is epitaxially deposited onto an N+ gallium arsenide slice. After the slice is polished, a thin film of silicon dioxide is reactively spluttered onto the surface to a thickness of approximately 6000 Angstroms. The wafer 330 with the N-type epitaxial layer 331 and the silicon dioxide surface layer 332 are shown in step (a).

55 By a photomasking technique, a hole 333 is then cut in the layer 332 as shown in step (b). The slice is then sealed in a quartz ampoule with $ZnAs_2$ and is diffused for about two minutes at $900^{\circ}C$. The result is shown in step (c) with the diffusion of zinc 334 through the hole 333 being accomplished. The depth of diffusion is of the order of about 0.3 mils. In addition to the diffusion through the hole 333, the zinc also 60 diffuses through the layer 332 to form a

thin P layer under the oxide. The oxide layer is then removed as shown in step (d). As shown in step (e), the slice is treated with a sulphuric acid etch to remove the thin P layer outside the regions defined by the hole 333. At this point, a new oxide layer 335 is sputtered onto the slice as indicated in step (f). By photomasking and selectively etching, the oxide layer 335 is removed over the zone occupied by the zinc diffusion 334, as indicated in step (g). A transmission line strip is then evaporated onto the slice and alloyed with the gallium arsenide to form the contact 336, as shown in step (h).

After the formation of the varactor junction, the upper half of the substrate 330 is masked and a conductor is alloyed to the lower unmasked portion to form layer 229. The masking is then removed and a 1 mil thick dielectric is deposited to form layer 339. Upon this substrate, conductors shown in Figure 14 are incorporated by photolithographic masking techniques. Gallium arsenide and intrinsic silicon are preferred as substrate materials. A yttrium-iron-garnet substrate may be employed for the multiplier network. Gold may be employed on silicon and aluminum on gallium arsenide as the conductive materials.

90 While a planar construction is shown in Figure 15, it will be recognized that other modes of fabrication may be employed for providing the multiplier network on the semiconductor substrate. In Figure 17 a mesa-type construction is shown in which a mesa is first formed on the substrate 330 to provide a site for the diode 321. An insulating layer 330a is then formed on the surface of the substrate 330 extending up along the slopes of the mesa for insulating the junction therein.

105 Thereafter, the conductive layer 329 will be formed over a portion of the surface of the substrate for forming the common plate for condensers 311, 314, 317, 319, 326 and 328. The thin layer 339 of high dielectric material is then formed over the conductive layer 329. Thereafter, the condenser plates and the strip line loops will be incorporated in the circuit configuration shown in Figure 14.

110 The parameters in the construction illustrated in Figures 14—17, in general, are distributed constants. Resonances will be present within the system, such as illustrated in the graph shown in Figure 18. Reactances in the resonant circuits are plotted as a function of frequency. The impedance of the circuit, as viewed from the terminals of the varactor 321, is illustrated by the chain-dotted lines 350. The reactance of the varactor diode 321 is plotted as the solid curve 351. The dotted curve 352 is the reciprocal of curve 351.

The circuit construction of Figure 14, as further detailed in Figures 15-17, operates such that the intersection of the reciprocal curve 352 and the reactance curve 350 occurs at the input frequency of 2.25 Gc and at the harmonic frequencies of 4.50, 6.75 and 9.0 Gc, respectively.

While Figure 1 illustrates an array of integrated circuits in the antenna module 14, one form of construction of the phase shift delay line is shown in Figure 19. The delay line plate 360 has three integrated circuit modules 361, 362, and 363 mounted thereon. Such a wafer may be included in the package shown in Figure 2.

The first module 361 may include the switches SW1 and SW2 of Figure 4. The module 362 will include the switches SW3 and SW4 and the module 363 will include switches SW5 and SW6. The delay lines 111-115 are formed on the plate 360 with the line length being progressively longer as by factors of 2, from one line to another. Plate 360 is provided with input transmission line terminals on the tab 365 for transmission to and from the plate 360 of the phase control carrier and received signal voltages as well as the clock pulses.

With integrated circuits 361-363 of form illustrated, the wafer 360 may be relatively small with maximum dimensions of the order of about an inch.

Figure 20 is illustrative of the construction of the integrated circuit wafer for the switching networks. The substrate 370 is of polycrystalline silicon. Insulation isolation cups 371, 372, and 373 surround and isolate islands 374, 375, and 376 of N-type material. The surface-oriented diode formed in the island 374 may be of the type illustrated in Figure 7 and will serve as either the transmit diode 122 or the receive diode 123 of Figure 4. A diffused N+ zone 377 is connected to a strip conductor 378 which is formed over a surface insulation layer 379. A diffused P+ zone 380 is then connected by conductor 381 to the emitter terminal of transistor 382.

A transistor 382 is formed of the N zone 375, P zone 383, and N+ collector zone 384. A conductor 385 connects the collector of the transistor 382 to a resistor 386, the resistor being formed by a P-type diffusion zone 387 in the N-type island 376. Lead 388 is connected to the resistor 386 and extends to other circuit elements.

With construction of the type illustrated in Figures 19 and 20, the phase shift delay lines and the control networks in integrated circuit form may be included in module 14. At some frequencies and for some applications, it will be desirable to construct phase shift modules separate from the radiation module 14. Such phase shift modules may be formed as shown in Figure 19 and

would be connected in the antenna circuit between the manifold 40 and the radiation module 14.

IF PREAMPLIFIER

The IF preamplifier of Figure 4 is of integrated circuit construction and has a gain of about 50 db. Such high-gain integrated circuit amplifiers operating at frequencies in the range from 200 Mc to the low Gc's, are subject to oscillation as a result of electromagnetically-coupled feedback within the integrated circuit package. This is primarily due to the very close spacing between the active and passive components formed integral with the semiconductor substrate.

Figure 21 illustrates an integrated circuit 410 of construction suitable for the IF amplifier 89 of Figure 4. The circuit 410 is comprised of a substrate 412 of single crystal, high resistivity silicon or other semi-insulating or high-resistance semiconductor material having first and second surfaces 414 and 416. The resistance required between the surfaces 414 and 416 will vary with the frequency at which the circuit is operated, the lower the frequency the greater the resistance required. However, for higher frequency applications, high resistivity semiconductor material is adequate. The components for the IF amplifier are formed at the surface of the semiconductor substrate 412 using any conventional technique. For example, a transistor 418 may be formed in the surface by sequentially diffusing N-type, P-type and N-type regions into the surface 416 of the substrate through openings etched in an oxide film 420. Alternatively the components may be formed on the surface of the substrate by epitaxial techniques. The circuit may also include interconnecting strip conductors such as 422, 423 and 424 which may be placed directly on the high resistivity substrate 412 or on the oxide film 420. The conductors may also form inductors such as indicated by the dotted outline at 426.

An insulating layer 428 is deposited over and adherently bonded to the portion of the second surface of the substrate 412 which is exposed and to the components of the circuit and is therefore integral with the substrate. Metalized films 432 and 434 are adherently bonded to the insulating layer 428 and to the first side 414 of the substrate. When the metalized films 432 and 434 are connected to ground, as represented by the conductors 436 and 438, the entire integrated circuit is disposed between two closely-spaced ground planes. As a result of the closely-spaced ground planes, the electromagnetic radiation from any particular component is attenuated by a loss factor of

$$\text{Loss} = k \left(\frac{d}{2s} \right) \text{db}$$

wherein k is dependent upon the dielectric constant of the material between the components and the respective ground planes, d is the distance from the point at which the electromagnetic wave is generated, and s is the spacing between the ground planes. Although the attenuation increases as the spacing between the ground plane decreases, the insulating layer 428 should be at least 1.0 mil thick and is preferably from 3—5 mils in thickness. It will be desirable to envelope the entire circuit structure, including the substrate and insulating layer, in the metalized ground plane.

In Figure 21 the insulating layer 428 is glass. The glass is selected so as to have a coefficient of thermal expansion closely matching that of the substrate so as to provide thermal-mechanical stability. Further, for stabilizing the high-frequency transmission lines, the insulating layer 428 is preferably about the same thickness as the substrate 412 so that the dielectric constant between the circuit components and each of the ground planes will be approximately equal. However, the insulating layer 428 may be any material which may be adherently bonded to the substrate 412, which is chemically compatible with the substrate and active components at various temperatures, and which has a thermal coefficient of expansion compatible with that of the substrate 412 so that the substrate will not be placed under stress due to temperature changes, and may be of any desired thickness, usually thin for amplifier application and relatively thick for transmission line application. The dielectric constant may be very closely matched by making the insulating layer 428 from high-resistivity semiconductor material of the same type as the substrate 412. This can be accomplished by epitaxial growth, if a single crystal is desired for part of an active component, or by another process where a polycrystalline structure will suffice. The substrate 412 should be relatively thin, for amplifier applications where it is desired to place the ground planes as close to the active components as practical, and will usually be less than about ten mils in thickness.

As an alternate structure, the substrate 412 may be a doped semiconductor material rather than intrinsic silicon or semi-insulating semiconductor material. In such case an insulating layer is provided between the metalized film 434 and the substrate so that the ground plane formed by the film 434 will be electrically insulated from the components of the circuit. Such an insulating layer may be any suitable material such as silicon dioxide, aluminum trioxide, glass, or the like, but is preferably glass. The device 50 is particularly suited for lower frequency

applications where the dielectric constant should be higher.

An IF amplifier or the like is fabricated on and in the surface of the substrate 412 using any conventional technique as heretofore described. Then the glass insulating layer 428 is formed by applying a liquid in which a high concentration of very fine glass particles is suspended. The glass particles are allowed to settle from the liquid and deposit as a sediment on the surface of the substrate and over the components of the circuit. The sedimentation process tends to deposit the glass particles over uniformly the components of the circuit and produce an essentially planar surface. Then the substrate is heated to a temperature sufficiently high to fuse the glass particles into a solid mass which adherently bonds to the exposed portion of the substrate, the oxide insulating film 420, if any, or the components of the circuit, as the case may be.

Although the insulating layer 428 was identified as glass applied by means of the liquid suspension technique, the insulating layer 428 may also be formed from glass or quartz which is evaporated in a high vacuum and condensed on the surface of the substrate. The metalized films 432 and 434 may then be deposited by a conventional evaporation and condensation process.

The exposed surfaces of the substrate and insulating films are then metalized, preferably by evaporating and condensing a metal onto the surfaces, or by other well-known techniques. Gold, aluminum or other suitable metal may be used for this purpose. However, if gold is to be deposited directly on a silicon substrate, a thin layer, a few angstroms thick, of molybdenum or other metal which does not dope the silicon is preferably deposited on the surface 414 before the gold is deposited to prevent doping of the silicon by the gold.

The integrated amplifier circuit is disposed between a pair of closely-spaced ground planes. The ground planes and the circuit are interconnected so as to provide a rugged, sealed package. For high frequency transmission lines, the dielectric properties between the circuit components and each of the ground planes may be made approximately equal for improved performance.

BEAM STEERING REFERENCE VOLTAGE GENERATION

Where the antenna is made up of an array of elements arranged in rows and columns as shown in Figures 22 and 23, each of the rows and columns may be numbered for convenience according to their position in the array. To shift the beam of the antenna in a horizontal direction through an angle ϕ , Figure 22, the phase of the RF energy applied to the radiation structure in each

module in each column must be shifted by an amount which is proportional to the angle ϕ , the angle that the beam is to be shifted from a line perpendicular from the face of the antenna. The phase shift for each module must also be dependent upon the location of the module in the array. Figure 22 shows a top view of the antenna unit 12 and a plot of the phase shift versus distance from the centre of the antenna.

As shown in Figures 22 and 23, the control unit 510 generates a reference voltage which shifts the phase for the column $-n$ at the right edge of antenna 12 through the same phase angle. As represented by the tapped resistor 510a in unit 510, the voltages applied to the columns in the left antenna half are the same for each column but are graded from a maximum at the edge column to near zero at the centre column. The right antenna half columns similarly are controlled by reference voltages such as might be derived from resistor 510b. The unit 550 similarly serves to control the vertical scan or beam position. To point the beam in a direction involving both the horizontal and vertical deflection, the reference voltage for a given antenna element is the sum of the voltage required for the column in which a given element is positioned and the voltage required for the row in which the given element is located. Thus, as illustrated in Figure 23, the column at the right side of the antenna unit 12 would be delayed by an angle $-\phi$. The column at the left edge of the antenna unit 12 would be delayed by an angle of $+\phi$.

Where the antenna array is one wavelength wide and where the difference between the angle $-\phi$ and $+\phi$ is 360° , the antenna radiation primarily will be at 45° to the face of the antenna. In practice, however, the antenna generally is made many wavelengths wide as well as high so that narrow beams may be produced. When this is done, it is necessary to produce phase shifts across the face of the antenna which are equal to $N2\pi^\circ$. The factor N may be any integral number with practical values ranging as high as 10 to 15 or more for phase shifts of around 5000° across the antenna.

In Figure 24 the controller for generating the horizontal and vertical reference voltages above noted is shown, with the controller for producing the horizontal reference voltages being shown in detail.

In order to point the beam in a given direction, a binary number, proportional to the phase shift required for the edge column n , Figure 22, is read into an input register 511 of unit 510 from a control source 510c. The register 511 is connected to a switch unit 512. A reference voltage is applied to the switch 512 by way of an input channel 513. The digital-to-analog converter of

Figure 24, including switch unit 512, may be the same as in Figure 4 which shows the construction of the switch units SW1—SW6 and the connections to the ladder network. The register 511 may be composed of bistable elements as shown in Figure 4 or may comprise other binary storage elements. These elements control switches in unit 512 which in turn control the binary weighted resistance ladder of the type commonly used in digital-to-analog converters. Typical of the construction is the resistance network illustrated in the unit 514. The resistance values are chosen so that the voltage at the output is one-half the value of the reference voltage on terminal 513 when switch S1 is closed to the reference voltage and all the other switches are closed to ground. When switch S2 is closed to the reference voltage and all the other switches are connected to ground, the output voltage is one-fourth the reference voltage, etc. This assumes that the series resistances 514a are not present. Resistances 514a, however, are included for the purpose which will later be explained. In operation the switch for each given ladder position is connected to the reference voltage if the bit in the corresponding register is 1, and to ground if the bit is 0.

The output of the ladder network 514 is applied by way of conductor 515 to a second digital-to-analog unit including switch unit 516 which controls a ladder network 517 and which in turn is controlled by a counter 518. A second counter 519 counts in parallel with counter 518. A decoding logic network 520 is connected to counter 519. Counters 518 and 519 are controlled by a clock 521 which is connected thereto by way of an AND gate 522 and line 527. A control multivibrator 523 controls one input of the AND gate 522. The decoding logic network 520 has output lines i to n with output lines n being connected by way of line 524 to the reset terminal of the multivibrator 523.

A starting unit 525 is connected to the start terminal of the multivibrator 523. The starting unit 525 is also connected to the reset terminal of counter 519 and, by way of an AND gate 526, to the reset terminal of the counter 518.

One control terminal of the AND gate 526 is connected to the output of a comparator 528 which is connected at one input to the output line 529 of the ladder network 517 and at the other input to a comparison reference voltage source 530.

The line 529 is also connected to a bus 531 at the input of a plurality of sample-and-hold units 532i—532n. Line 529 is connected by way of an inverting unit 540 to a bus 541 to sample-and-hold units 542i—542n.

The voltages appearing at the outputs of

the sample-and-hold units 432i—532n and 542i—542n are the voltages necessary to shift the beam from antenna unit 12 through a horizontal angle represented by the reference voltage from the numerical input unit 510c.

In a similar manner, a vertical control voltage generator 550 provides output voltages to sample-and-hold units 552i—552n and 562i—562n for shifting the beam from the antenna unit 12 through a vertical angle representative of the magnitude of the reference voltage applied from the reference numerical input voltage source 550c. The voltages from the sample-and-hold units may then be combined for application to the reference input terminals of each module (terminal 35 of Figure 4), so that each module in the antenna unit will be adjusted to shift the phase of the RF antenna excitation pulse in dependence upon the sum of the vertical and horizontal beam angles represented by the voltage on units 510c and 550c. The voltages may be combined from the sample-and-hold units in the manner known in the art, and such as described in "Introduction to Radar Systems", Skolnik, McGraw-Hill (1962), page 312 et seq.

In operation, where a scanning sequence of the antenna is desired, the numbers to be read into the units 510 and 550 from the control sources 510c and 550c come from sequence generators or programmers. The units 510c and 550c may comprise part of a computer if the antenna is to be pointed at some target, as would be the case in a target tracking operation. In either case the voltage output on line 529 will then be proportional to the phase shift desired in the extreme or edge columns of the antenna.

As soon as the phase shift number or signal has been read into the unit 510, a start pulse is applied to the control multi-vibrator 523. This pulse also resets the counters 518 and 519. As soon as the control unit 523 is set, the AND gate 522 changes state to allow the clock pulse train to pass to the counters 518 and 519. This causes the two counters to advance together. The counter 518 controls the units 516 and 517, with the reference input voltage being the voltage on line 515. As the count in the counter 518 increases, the voltage on line 529 increases in uniform steps.

In the explanation of operation of the reference generator which follows, it will first be assumed that the total phase shift across the face of the antenna is to be less than 360°. Thereafter, operation for a phase shift greater than 360° will be explained.

For a phase shift less than 360°, counter 519 will count in synchronism with counter 518. The state of counter 519 is decoded to provide n indications on n individual output lines 520i—520n. The output voltage

on line 529 for each step of counters 518 and 519 is a voltage proportional to the phase shift for each column. That is to say, the first state of counters 518 and 519 results in a voltage proportional to the phase shift for columns $+i$ and $-i$ of Figure 23. The second state of counters 518 and 519 results in a voltage for columns $+ii$ and $-ii$, and so on. It will be noted from Figure 22 that the phase required for column n is the negative of the phase required for column $-n$.

Counters 518 and 519 initially are reset to a state of all zeros. This results in a ladder output voltage on line 529 of zero volts for the first state of counters. If the number of columns in the antenna is an even number, as shown in Figures 1 and 23, a reference of zero volts would result in the phase shift introduced in columns i and $-i$ always being zero. This would induce a slight discontinuity in the phase slope across the antenna. To prevent this, the ladder network 514 is provided with resistors 514a. These resistors offset the output of the ladder 514 by an amount equal to one-half step of the output voltage.

The lines 520i—520n, connected to the sample-and-hold units 532i—532n, are sequentially energized to cause storage of a sample voltage in each of the units as the states of the output lines leading from decoder 520 change. Similarly, the other half of the antenna is provided with reference voltages from bus 541 by way of inverter unit 540.

When the output on line 529 equals the reference voltage from source 530, as applied to the comparator 533, the counter 518 is reset. Decoder 520 serves to reset counter 519 but only at the end of a phase control sequence. The voltage from reference source 530 is set at a value corresponding with just less than the voltage on line 529 required for 360° phase shift.

Thus far, it has been assumed that the total phase shift required is less than 360°. This generally is not the case and this fact is the basis for including the second counter 519. More particularly, with the output from the voltage ladder 517 fed to the comparator 533 and with the reference voltage from source 530 slightly less than the voltage necessary for a 360° phase shift, when the ladder output voltage exceeds the voltage from source 530, the counter 518 will be reset. However, with the clock pulse being applied thereto, counter 518 will repeat its cycle so long as the clock pulse train is present. In contrast, the counter 519 continues its count until the clock pulse train is stopped by disabling gate 522. In this way, the output of the ladder 517 always indicates a phase shift in the range of 0° to 360°. Counter 519 always contains the

number of the columns in binary form for which the voltage being generated at that instant applies.

The sample-and-hold units may be of conventional construction involving closure of a switch in response to a given voltage state on a decoder output line, such as line 520i. This charges a capacitor in the sample-and-hold unit 532i such that the voltage on the output line from unit 532i is equal to the input voltage on bus 531 at the instant of closure of the switch. With a high impedance output buffer-amplifier in the sample-and-hold units, the charge on the condenser will remain unchanged after the input switch is opened. Switches in the sample-and-hold units are controlled by the decoded state of counter 519, as above noted. State 1 of counter 519 closes the switch in the sample-and-hold units 532i and 542i. Since the inverter 540 is employed to feed bus 541, the two voltages are thus stored as reference voltages for two phase shift units. When the counter 519 reaches its nth state, a voltage for each column is stored in the 2n sample-and-hold units. The decoded nth state of counter 519 also resets unit 523 and ends the process.

The controller 550 for the rows of antenna modules is identical to the controller 510 for the columns of antenna modules. If the rows and columns are the same in number, then the controllers are identical. If the rows and columns are not the same, then the controllers differ only in the number of states produced by the counter 519.

The phase shift reference voltage, for application to a given module, is produced by summing the voltages from two of the sample-and-hold units. This would be accomplished by means of a pair of summing resistances for each element, such as resistances 560 and 561. The output voltage from unit 552i would be separately summed with each of the output voltages from the sample-and-hold units 532i-532n and 542i-542n.

It is not necessary that the antenna be as shown in Figure 23. By omitting elements in the outer rows or columns, the configuration shown in Figure 1 may be formed. Entire rows or entire columns may be omitted depending upon the particular application required. If only one column is employed or if only one row is employed, then either the unit 510 or the unit 550 would be employed to generate the phase control reference voltages.

TIME SEQUENCE

In Figure 25 Time Graphs I-XII illustrate the operation of the system. Graphs I-V represent the operation of the delay line phase control network and Graphs VI-XII are system timing functions.

The voltage shown on Graph I represents the voltage at the input to the voltage comparator 143, namely the reference voltage applied to terminal 235. The voltage of Graph II is a reset pulse applied to the counters (not shown) to reset the circuits including switches SW1-SW6 to zero upon the appearance of a reference voltage at terminal 35 which is changed from any previous value.

The voltage on Graph III represents the voltage at the output of the converter 153 and applied to the voltage comparator 143. This voltage appears on line 154.

The wave form shown on Graph IV represents the output voltage appearing at the output of the voltage comparator 143. The voltage represented by Graph V represents the output pulses passing through the AND gate 142 and appearing on the input line 140 to the SW-1, which is the first stage in the 9-bit binary counter.

In operation, when the phase shift counter is reset, the output voltage from the analog converter 153 drops back to zero and then as the delay lines are switched into the circuit by operation of the switches SW1-SW6, the voltage on line 154 builds up until it equals the value of the reference voltage on terminal 35 at which time the switching circuit ceases to change state by reason of the fact that the AND gate 142 is then disabled.

Graph VI illustrates the state of the transmit-receive switches. More particularly, the voltage of the master trigger shown on Graph VI is applied to the control input terminal of the multivibrator 163. The master trigger pulse actuates a gate circuit so that transmit switches 163, 137 and 120 will be conductive and receive switches 164, 138 and 121 will be nonconductive. During the remainder of each TR cycle, the receive switches 164, 138 and 121 will be conductive.

Graph VII illustrates the variation in the frequency control voltage generated by the pulse generator 44 of Figure 3. The frequency control voltage is applied to the oscillator 41 to vary the frequency from a low frequency to a high frequency over a band of 1.25 mc. The resultant output of the oscillator 41 is illustrated by Graph VIII. The modulated pulse appears at the output of the power amplifier frequency modulated over a range of 1.25 mc. However, as the antenna excitation voltage pulse appears at the output of the frequency multiplier, the modulation range is 5 mc.

Graph IX represents the variation in the gain of the receivers 56 and 57 of Figure 3. The gain is controlled by the sensitivity time control unit 67, Figure 3. Thus, at the beginning of the listening interval,

which is coincident with the onset of the transmitted pulse, the gain is gradually reduced, reaching a minimum level at a time coincident with the end of the transmitted pulse. The gain then is gradually increased as the radar range increases with time to a maximum value at the onset of the next transmitted pulse.

Graph X illustrates the received pulse delayed in time from the transmitted pulse. The received pulse is a compression modulated pulse appearing at the output of the IF amplifiers 56 and 57. The signal is then applied to the pulse compression filters 58 and 59, Figure 3, by which means the low frequencies are delayed a greater interval than the high frequencies so that the total energy of the received pulse is compressed, by a ratio of the order of 100 to 1, into a discrete pulse or energy bundle. Operation of a pulse compression filter generally speaking is characterized by a time delay T_d . Thus the computer timing pulse appearing on Graph XII is delayed by a like interval so that the radar range is represented by the time interval T_r .

The foregoing sequence is carried out for the selected values of the reference voltages applied to the input terminal 35 of Figure 4. Various programs may be followed to shift the beam from one direction to another at rates and in patterns which are dependent upon the requirements placed upon the system. It will be obvious that the template system above discussed may be used alternately with ground mapping programs and with air to air ranging programs by appropriate programming of the generator of Figure 23 which supplies the reference voltages.

The surface-oriented diode illustrated in Figures 5—11 is described and claimed in copending Patent Application Number 36403/65 (Serial No. 1,124,264).

The strip-line transmission line illustrated in Figures 6, 7 and 12 is described and claimed in copending Patent Application Number 36404/65 (Serial No. 1,124,265).

It is an advantage of the embodiment of the invention hereinbefore described that the construction lends itself to a lightweight multi-element array antenna using electronic beam scanning, eliminating wave guides, rotary joints, motors, synchros, gears, and other servo components normally essential to a scanning system. A substantial reduction in total volume and weight over known or existing radars is achieved. This is accompanied by a substantial increase in the reliability of the system.

It is a further advantage that each individual antenna module with individual power generation and phase control permits electronic beam steering. The use of

solid-state modules, together with microwave transistors, permits operation in the X-band and higher, and thus permits operation in that frequency range required for airborne radar. While the modules are capable of use in a wide variety of other radar installations, they are particularly suitable for airborne applications. Eliminated is the necessity for the magnetron, the local oscillator klystron, and for high power TR protection devices.

WHAT WE CLAIM IS:—

1. In a radar having an antenna formed by a multiplicity of modules each having radiation structure and forming substantially a planar radiation array each module including an RF unit, a phase shift unit, and a control network, the method which comprises:

- (a) applying a pulse of an RF carrier coincident in time and in phase to each of said modules,
- (b) simultaneously applying an in phase impulse of a phase control carrier to each of said modules,
- (c) shifting the phase of the phase control carrier pulse in each said module by phase angles dependent upon the position of each module in said array and in dependence upon a predetermined beam angle,
- (d) mixing each phase shifted phase control carrier pulse with the RF carrier pulse,
- (e) amplifying one of the modulation products from the combined phase control carrier pulse and the RF carrier pulse for excitation of said antenna,
- (f) sensing electromagnetic energy reflected to said antenna to produce a received signal in each module,
- (g) shifting said received signal in each module by a phase angle related to the shift in said phase control carrier pulse, and
- (h) combining all of the phase shifted received signals from said modules to produce an output signal.

2. A method according to Claim 1, wherein said outputs are registered as a function of time following the transmission of each pulse from said antenna.

3. A method according to Claim 1 or 2, wherein the frequency of said amplified modulation product is increased for excitation of said antenna at a higher frequency than said RF carrier.

4. A method according to Claim 1, wherein said amplified modulation product is multiplied by a factor of x for excitation of said antenna, said electromagnetic

which is coincident with the onset of the transmitted pulse, the gain is gradually reduced, reaching a minimum level at a time coincident with the end of the transmitted pulse. The gain then is gradually increased as the radar range increases with time to a maximum value at the onset of the next transmitted pulse.

Graph X illustrates the received pulse delayed in time from the transmitted pulse. The received pulse is a compression modulated pulse appearing at the output of the IF amplifiers 56 and 57. The signal is then applied to the pulse compression filters 58 and 59, Figure 3, by which means the low frequencies are delayed a greater interval than the high frequencies so that the total energy of the received pulse is compressed, by a ratio of the order of 100 to 1, into a discrete pulse or energy bundle. Operation of a pulse compression filter generally speaking is characterized by a time delay T_d . Thus the computer timing pulse appearing on Graph XII is delayed by a like interval so that the radar range is represented by the time interval T_r .

The foregoing sequence is carried out for the selected values of the reference voltages applied to the input terminal 35 of Figure 4. Various programs may be followed to shift the beam from one direction to another at rates and in patterns which are dependent upon the requirements placed upon the system. It will be obvious that the template system above discussed may be used alternately with ground mapping programs and with air to air ranging programs by appropriate programming of the generator of Figure 23 which supplies the reference voltages.

The surface-oriented diode illustrated in Figures 5—11 is described and claimed in copending Patent Application Number 36403/65 (Serial No. 1,124,264).

The strip-line transmission line illustrated in Figures 6, 7 and 12 is described and claimed in copending Patent Application Number 36404/65 (Serial No. 1,124,265).

It is an advantage of the embodiment of the invention hereinbefore described that the construction lends itself to a lightweight multi-element array antenna using electronic beam scanning, eliminating wave guides, rotary joints, motors, synchros, gears, and other servo components normally essential to a scanning system. A substantial reduction in total volume and weight over known or existing radars is achieved. This is accompanied by a substantial increase in the reliability of the system.

It is a further advantage that each individual antenna module with individual power generation and phase control permits electronic beam steering. The use of

solid-state modules, together with microwave transistors, permits operation in the X-band and higher, and thus permits operation in that frequency range required for airborne radar. While the modules are capable of use in a wide variety of other radar installations, they are particularly suitable for airborne applications. Eliminated is the necessity for the magnetron, the local oscillator klystron, and for high power TR protection devices.

WHAT WE CLAIM IS:—

1. In a radar having an antenna formed by a multiplicity of modules each having radiation structure and forming substantially a planar radiation array each module including an RF unit, a phase shift unit, and a control network, the method which comprises:
 - (a) applying a pulse of an RF carrier coincident in time and in phase to each of said modules,
 - (b) simultaneously applying an in phase impulse of a phase control carrier to each of said modules,
 - (c) shifting the phase of the phase control carrier pulse in each said module by phase angles dependent upon the position of each module in said array and in dependence upon a predetermined beam angle,
 - (d) mixing each phase shifted phase control carrier pulse with the RF carrier pulse,
 - (e) amplifying one of the modulation products from the combined phase control carrier pulse and the RF carrier pulse for excitation of said antenna,
 - (f) sensing electromagnetic energy reflected to said antenna to produce a received signal in each module,
 - (g) shifting said received signal in each module by a phase angle related to the shift in said phase control carrier pulse, and
 - (h) combining all of the phase shifted received signals from said modules to produce an output signal.
2. A method according to Claim 1, wherein said outputs are registered as a function of time following the transmission of each pulse from said antenna.
3. A method according to Claim 1 or 2, wherein the frequency of said amplified modulation product is increased for excitation of said antenna at a higher frequency than said RF carrier.
4. A method according to Claim 1, wherein said amplified modulation product is multiplied by a factor of x for excitation of said antenna, said electromagnetic



energy reflected to said antenna is detected to produce an IF signal in each module having a frequency of x times the frequency of said phase control carrier, and said IF signal in each module is shifted by a phase equal to x times the shift of said phase control carrier pulse.

5. In a radar having an antenna formed by a multiplicity of modules, each having radiation structure and forming substantially a planar radiation array each module including an RF unit, a phase shift unit, and a control network, the method which comprises:

- (a) applying RF carrier pulses and power to said modules,
- (b) shifting the phase angle of the RF carrier pulses in each of said modules with patterned gradation across said array related to the position of a given module in said array and related to a predetermined antenna beam angle,
- (c) amplifying the phase shifted RF carrier pulses to produce RF carrier pulses of enhanced power,
- (d) multiplying the frequency of the amplified RF carrier pulses, and
- (e) converting the resultant signals into electromagnetic radiation beamed from said array in dependence upon said patterned gradation.

6. In a radar having an antenna formed by a multiplicity of modules, each having radiation structure and forming substantially a planar radiation array each module including an RF unit, a phase shift unit, and a control network, a method which comprises:

- (a) controlling the phase of an RF signal having a relatively low frequency in accordance with the position of an element in the array,
- (b) amplifying the controlled phase RF signal to enhance the power to a level in excess of the power to be applied to the radiation element,
- (c) multiplying the amplified RF signal to produce a signal in the desired frequency band, and
- (d) exciting the element with the multiplied RF signal.

7. A method as claimed in Claim 6 wherein the RF signal has a frequency less than the X-band, and the multiplied RF signal has a frequency at least in the X-band.

8. A radar having an antenna formed by a multiplicity of modules forming substantially a planar radiation array, each of said modules comprising:

- (a) a radiation structure,
- (b) a solid state mixer and power amplifier connected in series between an RF input terminal and the radiation structure for pulsed excitation of the the radiation structure,
- (c) a variable phase shift circuit connected between a phase control carrier terminal and the mixer for controlling the phase of the pulse applied to the radiation structure,
- (d) a frequency multiplier circuit for increasing the frequency of the signal from the RF input terminal to the radiation structure, and
- (e) a receiving channel leading from said radiation structure and through the phase shift circuit to an output terminal.

9. A radar as claimed in Claim 8, wherein said frequency multiplier circuit includes capacitors, inductors and a variable capacity diode which circuit comprises:

- (a) a thick dielectric substrate having a first conductive layer on one surface thereof forming a ground plane,
- (b) a variable capacity diode formed at the other surface of the substrate,
- (c) a second conductive layer over a portion of the other surface of the substrate,
- (d) a thin high dielectric layer over the second conductive layer,
- (e) a plurality of conductive plates separated from second conductive layer by a thin, high-dielectric layer to form a plurality of capacitors, and
- (f) a plurality of narrow conductive strips interconnecting the plurality of conductive layers and the diode and extending beyond the margin of the second conductive layer over the other surface of the substrate to form inductors.

10. A radar as claimed in Claim 9, in which the plurality of conductive layers includes a plurality of plates shadowing another plate to form a series capacitance.

11. A radar as claimed in Claim 9, in which the multiplier is comprised of:

- (a) an inductor-capacitor low pass filter network means at the input for passing an input frequency,
- (b) an inductor-capacitor variable capacity diode resonant network means connected to the low pass filter network means tuned to resonate at the input frequency, and
- (c) an inductor-capacitor band pass filter network means connected to the



resonant network means tuned to pass only a multiple of the input frequency.

12. A radar as claimed in Claim 12 wherein the multiplier includes:

- (a) an inductor-capacitor impedance matching network means connected to the low pass filter network means and forming the input for the device, and
- (b) an inductor-capacitor impedance matching network means connected to the band pass filter network means and forming the output of the device.

13. The radar as claimed in Claim 9, wherein the resonant network circuit means is tuned to resonate at multiples of one, two, three and four of an input frequency and the band pass filter means is tuned to pass the fourth multiple frequency.

14. The radar as claimed in Claim 9, wherein said substrate is an intrinsic silicon semiconductor substrate having a ground plane conductor on the bottom thereof.

15. The radar according to Claim 9, wherein said plurality of conductive strips loop from said plates over the top of said substrate beyond the margin of said conductive film to form inductors to interconnect said plates.

16. The radar according to Claim 9, wherein said multiplier circuit is a high frequency integrated circuit device formed in a semiconductor wafer having a pair of opposed major faces which are substantially planar, the bulk of the wafer being substantially intrinsic with one of the major faces including a first continuous high conductivity layer and the other of said faces including a fractional portion of its area covered by a second continuous high conductivity layer, a thin high dielectric layer over said second layer, a strip line signal path comprised of thin conductive strips and thick conductive strips connected in series, said thick strips being positioned on said dielectric layer and said thin strips extending over said wafer outside the margins of said dielectric layer, and a varactor diode formed on zones of opposite conductivity type, one of which is at the other of said faces forming a shunt path between said strip line and said first layer, said diode being connected at one terminal to a point on said strip line outside the margin of said dielectric layer.

17. A radar according to Claim 8, wherein said phase shift circuit is a digitally-variable length delay line circuit for producing a phase shift in an A.C. signal proportional to an input reference signal which circuit comprises:

- (a) a plurality of strip-line conductors of digitally-increasing lengths,
- (b) a series of diode switching means for alternatively connecting each of the conductors in a series circuit or shunting the conductor to provide a digitally-variable length strip line,
- (c) a bistable multivibrator connected to operate each diode switching means,
- (d) control circuit means for actuating the bistable multivibrators sequentially in response to a clock pulse signal to provide a digitally-increasing effective line length,
- (e) converter means connected to the strip line for producing a feedback signal proportional to the effective line length,
- (f) a comparator connected to the output of the converter means for comparing said feedback signal to a reference input signal related to the desired phase angle and for producing an output signal when the reference input signal exceeds the feedback signal by a predetermined amount, and
- (g) an AND gate connected at its output to the input of a bistable multivibrator and connected at its inputs to the output of the comparator and to a clock pulse terminal for passing clock pulses only when the comparator produces its output signal.

18. A radar having an antenna formed by a multiplicity of modules, each having radiation structure and forming substantially a planar radiation array comprising:

- (a) means to provide separate first signals of like frequency and phase for each of said modules,
- (b) means within each of said modules to multiply the frequency of said first signal thereby to provide a second high frequency signal within said module, and
- (c) means to impose a separately-controllable phase shift upon each of said first signals prior to frequency multiplication thereof.

19. A radar having an antenna formed by a multiplicity of modules substantially as hereinbefore described with reference to Figures 1 to 6, and 13 to 16, and 21 and 25 of the accompanying drawings.

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