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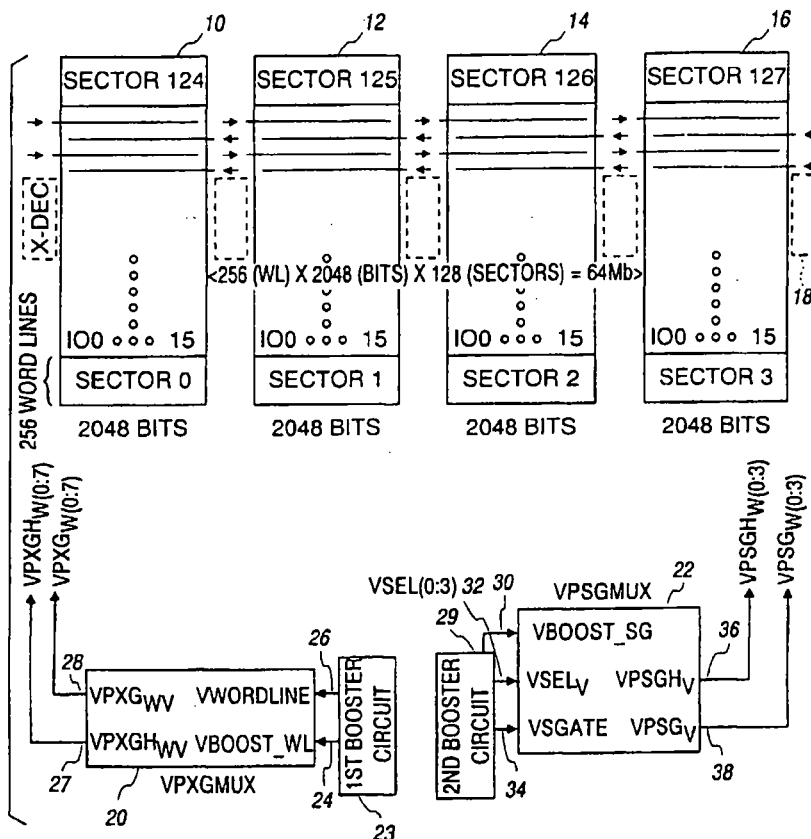
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(54) Title: METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES



(57) Abstract: An apparatus and a method for reducing capacitive loading in a Flash memory X-decoder so as to accurately control the voltages at selected wordlines and block select lines are provided. A decoding structure (18) separately applies a first boosted voltages to the wordline N-well region and a second boosted voltage to the selected wordline so as to reduce capacitive loading on the selected wordline due to heavy capacitive loading associated with the wordline N-well region. The decoding structure further applies a third boosted voltage to the select gate N-well region and a fourth boosted voltage to the block select line so as to reduce capacitive loading on the block select line due to heavy capacitive loading associated with the select gate N-well region. As a consequence, an accurate voltage can be created quickly at the selected wordline since its capacitive loading path is very small.

WO 01/97230 A3



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WO 01/97230 A3

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