FIG. 1

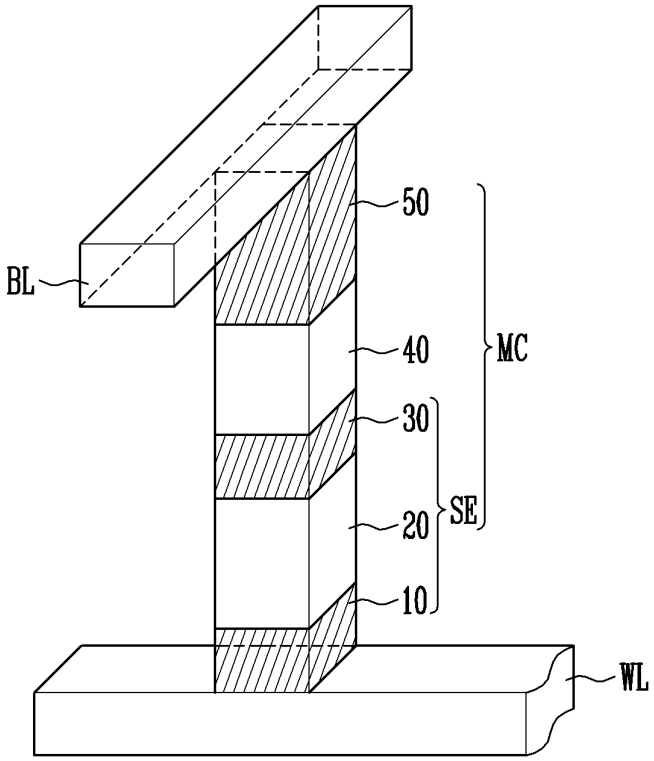


FIG. 2

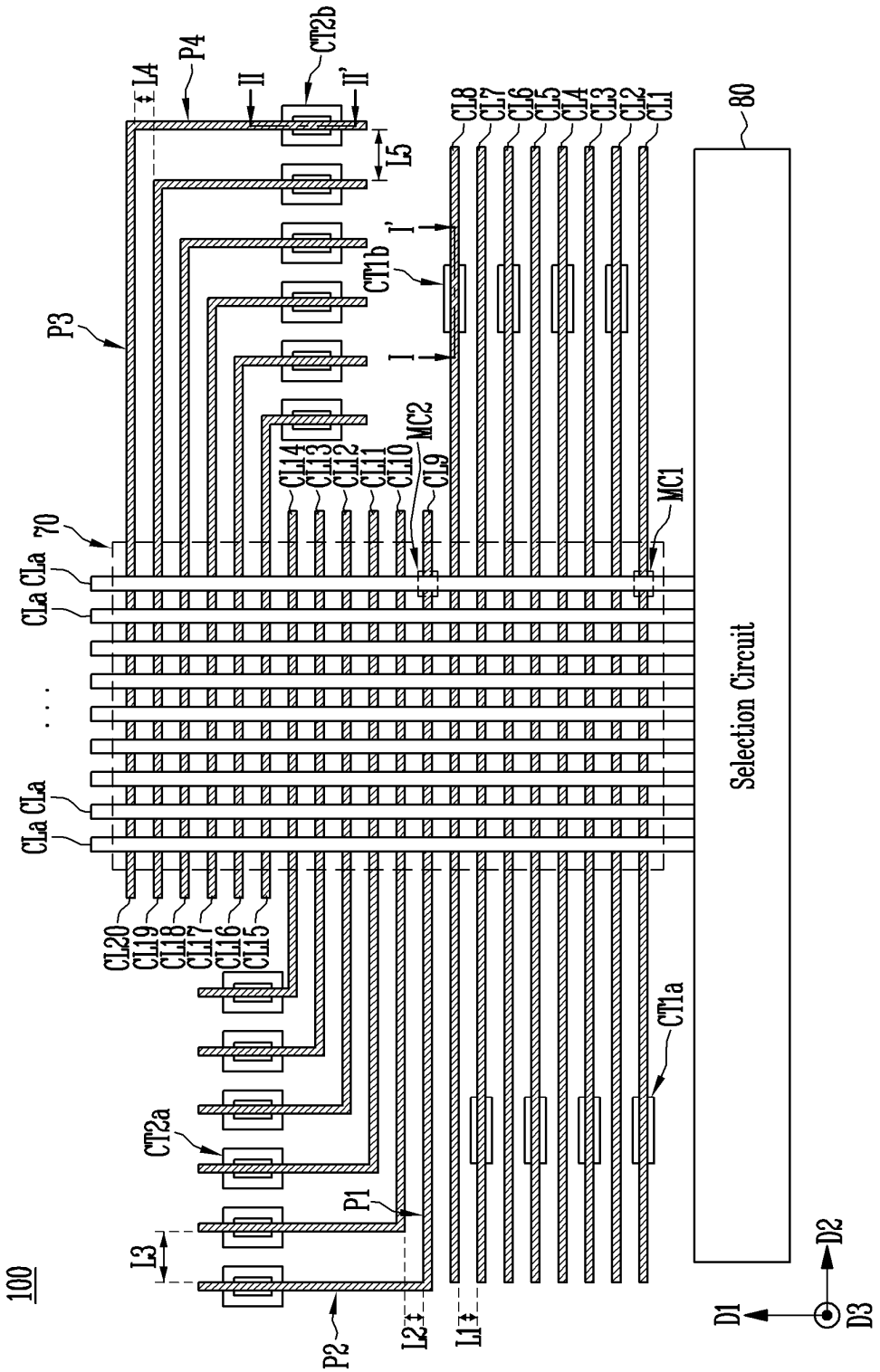

100
P1
P2
P3
P4
L1
L2
L3
L4
L5
II
II'
I
I'
CT1a
CT1b
CT2a
CT2b
MC1
MC2
70
80
CLa
CL1
CL2
CL3
CL4
CL5
CL6
CL7
CL8
CL9
CL10
CL11
CL12
CL13
CL14
CL15
CL16
CL17
CL18
CL19
CL20
Selection Circuit
D1
D2
D3

FIG. 3

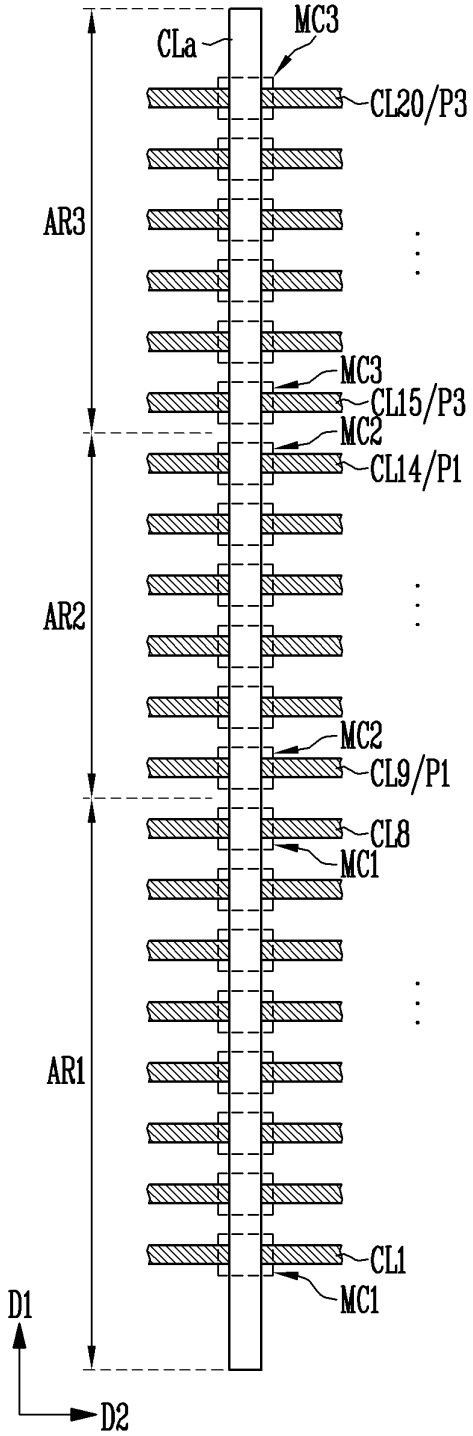

CLa
MC3
CL20/P3
AR3
MC3
CL15/P3
MC2
CL14/P1
AR2
MC2
CL9/P1
CL8
MC1
AR1
CL1
MC1
D1
D2

FIG. 4A

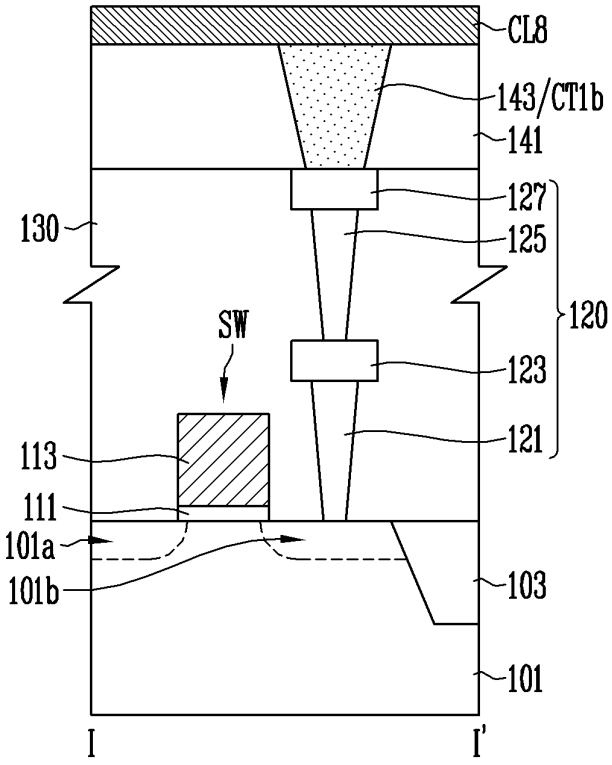

CL8
143/CT1b
141
127
125
130
120
SW
123
121
113
111
101a
101b
103
101
I
I'

FIG. 4B

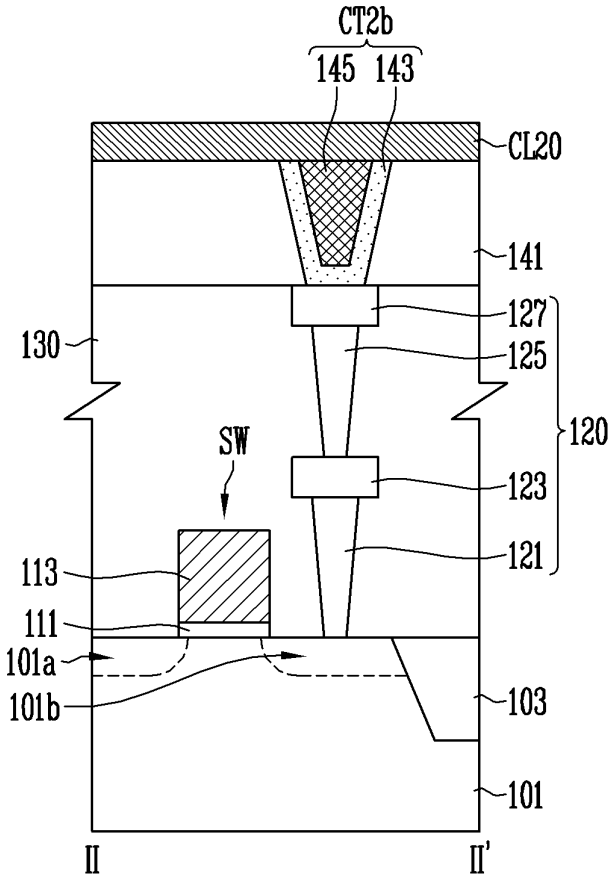

CT2b
145
143
CL20
141
127
130
125
120
SW
123
121
113
111
101a
101b
103
101
II
II'

FIG. 5

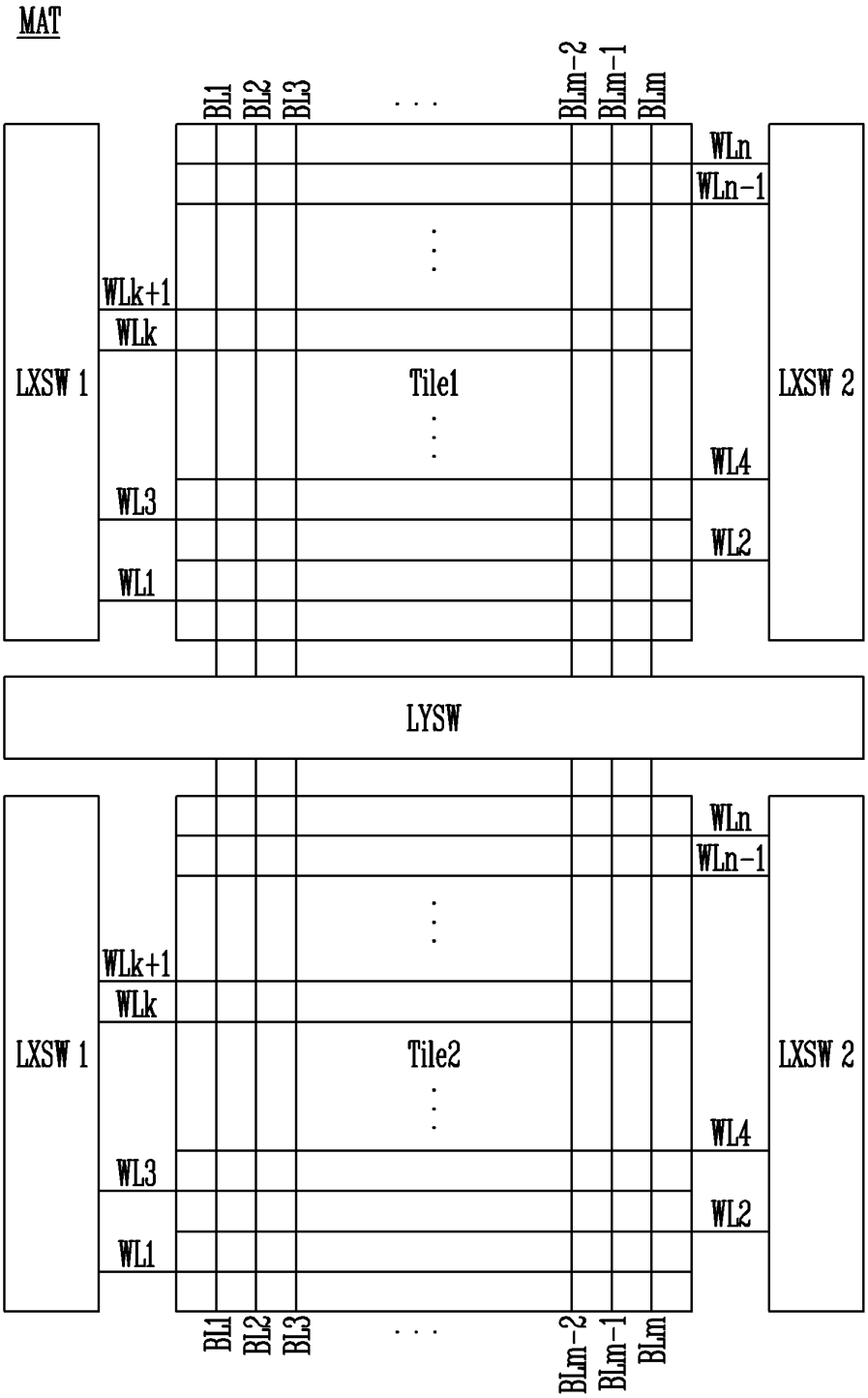

MAT
BL1
BL2
BL3
BLm-2
BLm-1
BLm
WLn
WLn-1
WLk+1
WLk
LXSW 1
Tile1
LXSW 2
WL4
WL3
WL2
WL1
LYSW
WLn
WLn-1
WLk+1
WLk
LXSW 1
Tile2
LXSW 2
WL4
WL3
WL2
WL1
BL1
BL2
BL3
BLm-2
BLm-1
BLm

FIG. 6

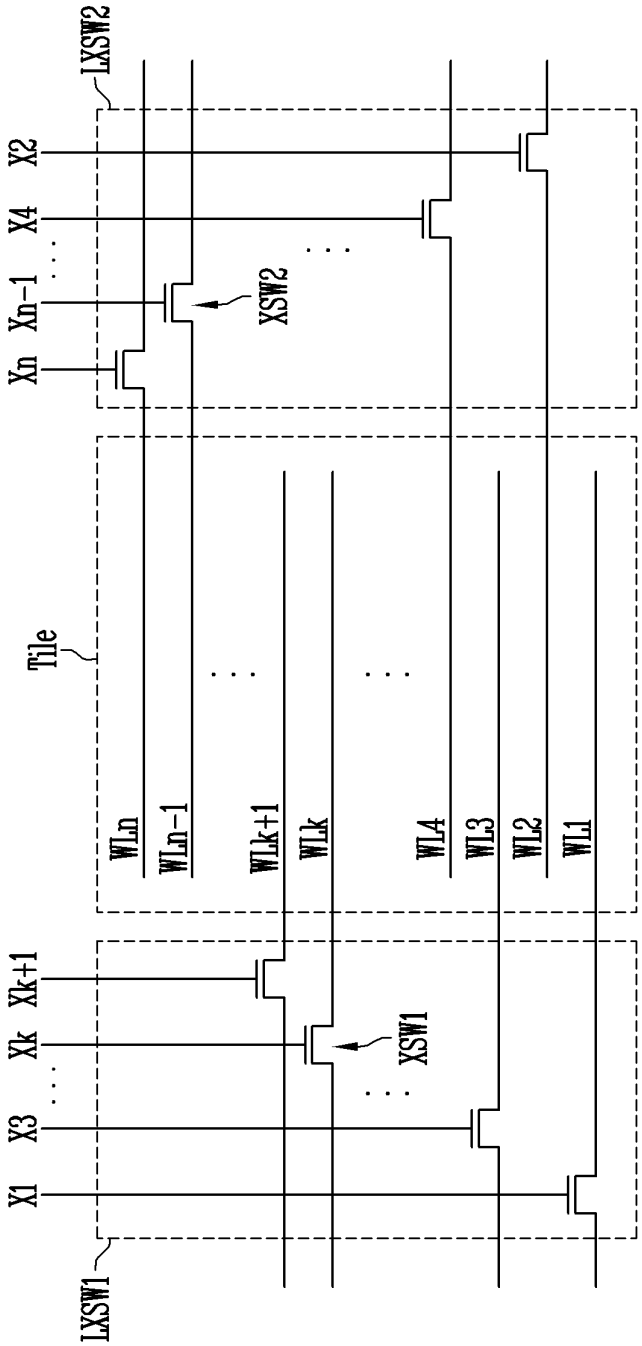

LXSW2
X2
X4
Xn-1
Xn
XSW2
Tile
WLn
WLn-1
WLk+1
WLk
WL4
WL3
WL2
WL1
Xk+1
Xk
X3
X1
XSW1
LXSW1

FIG. 7

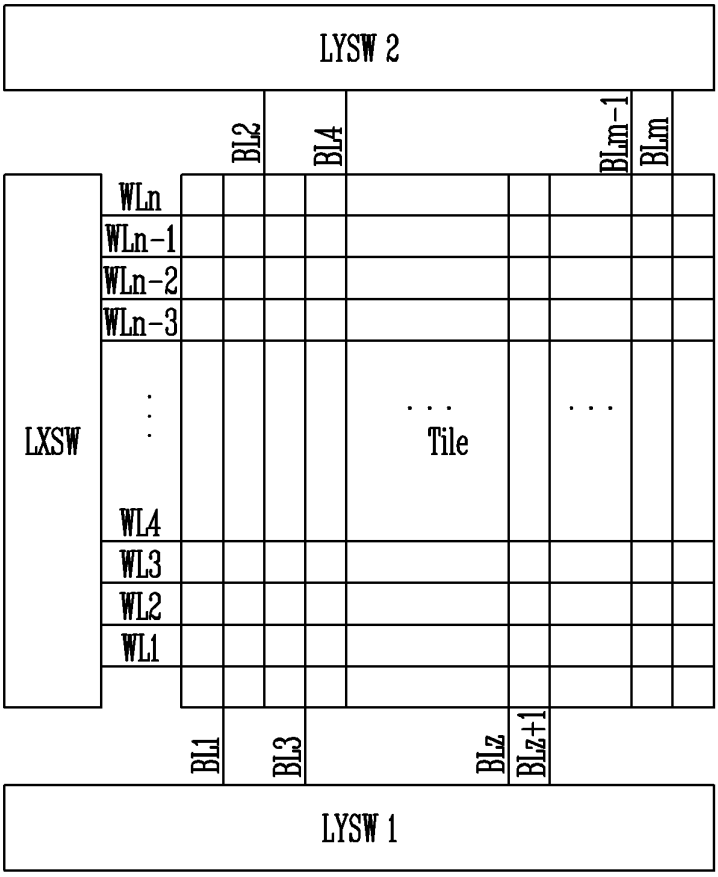

LYSW 2
BL2
BL4
BLm-1
BLm
LXSW
WLn
WLn-1
WLn-2
WLn-3
WL4
WL3
WL2
WL1
Tile
BL1
BL3
BLz
BLz+1
LYSW 1

FIG. 8

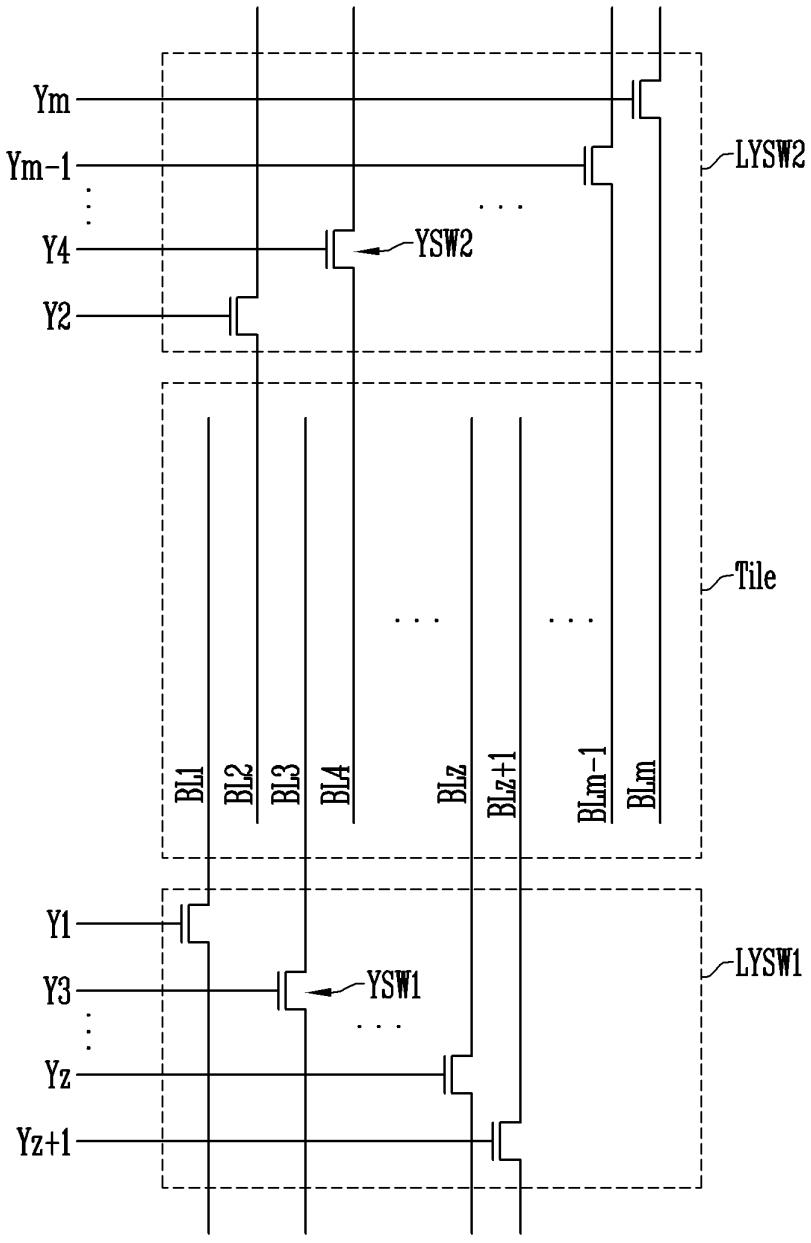

Ym
Ym-1
Y4
Y2
YSW2
LYSW2
Tile
BL1
BL2
BL3
BL4
BLz
BLz+1
BLm-1
BLm
Y1
Y3
Yz
Yz+1
YSW1
LYSW1

FIG. 9A

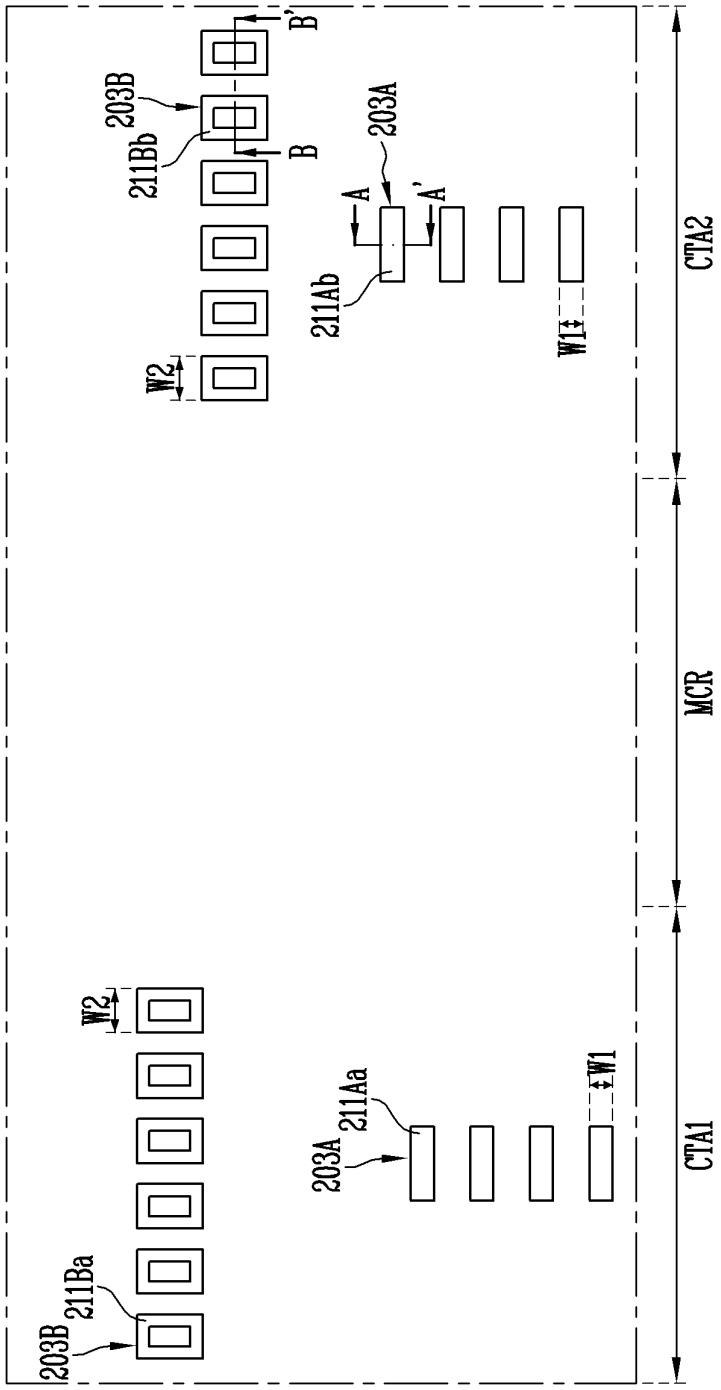

CTA2
MCR
CTA1
B'
B
A
A'
203B
211Bb
203A
211Ab
W2
W1
W2
W1
203A
211Aa
203B
211Ba

FIG. 9B

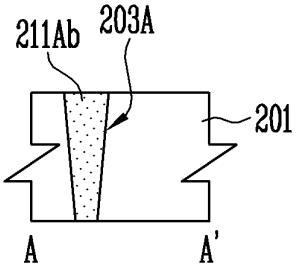


FIG. 9C

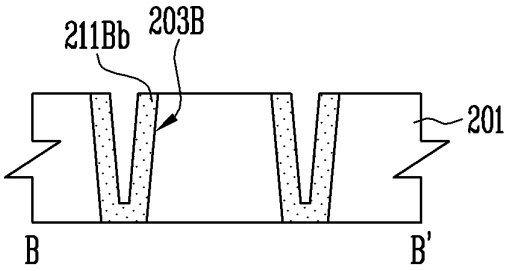


FIG. 10A

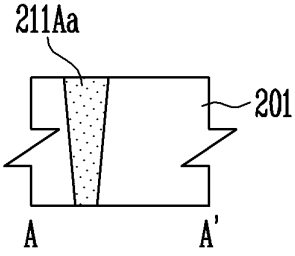


FIG. 10B

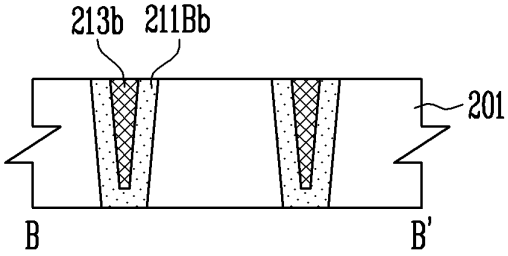


FIG. 11A

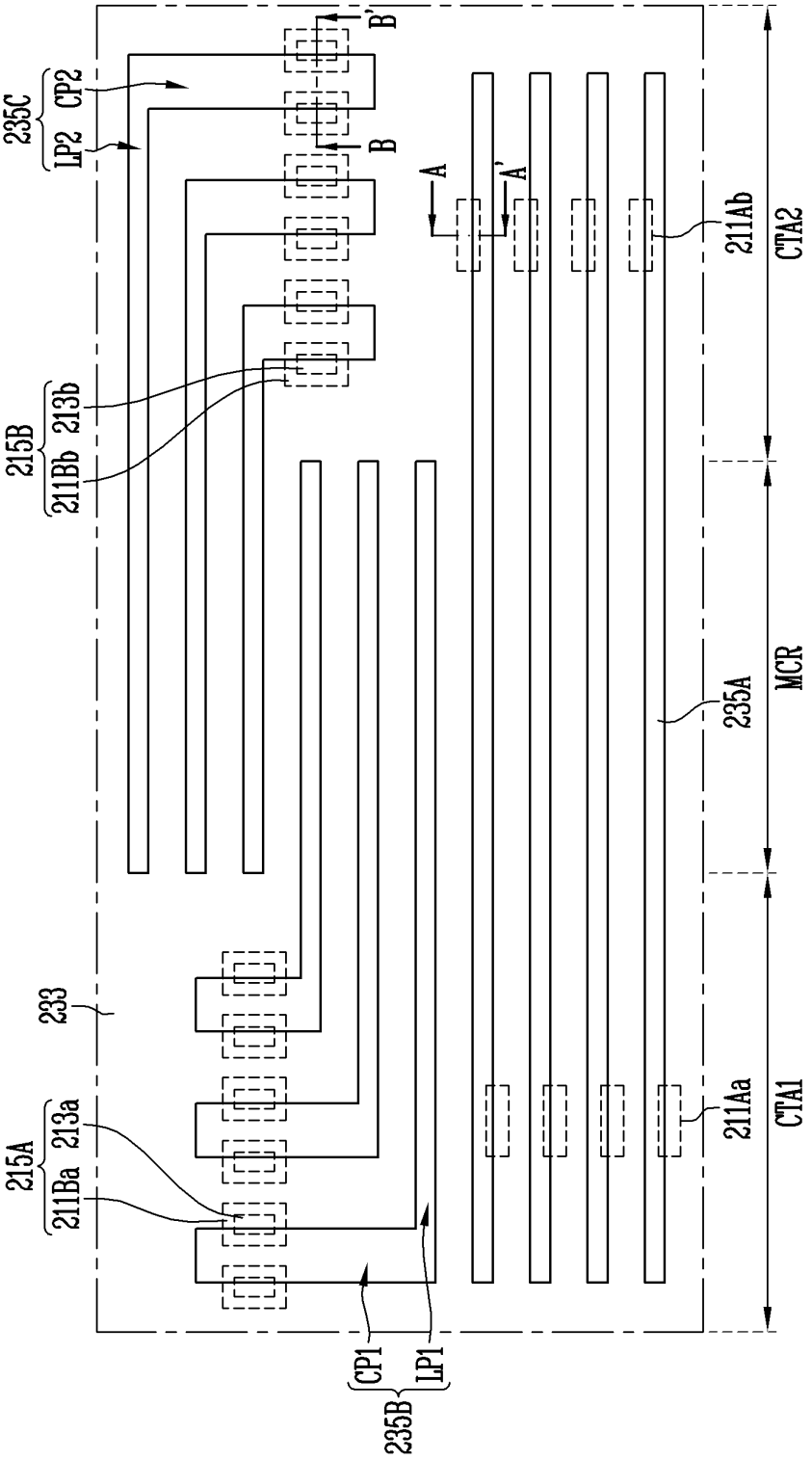

235C
CP2
LP2
215B
213b
211Bb
215A
213a
211Ba
233
235B
CP1
LP1
235A
211Aa
211Ab
CTA1
MCR
CTA2
A
A'
B
B'

FIG. 11B

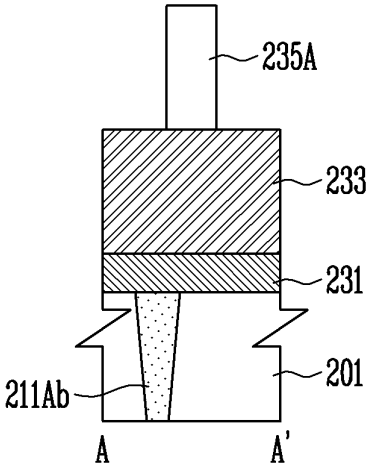


FIG. 11C

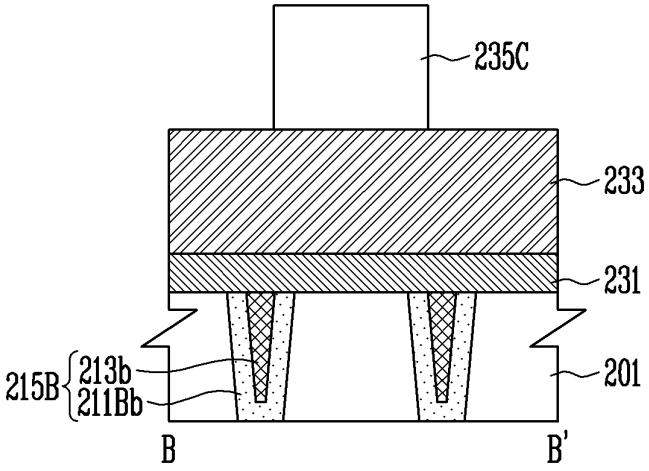


FIG. 12A

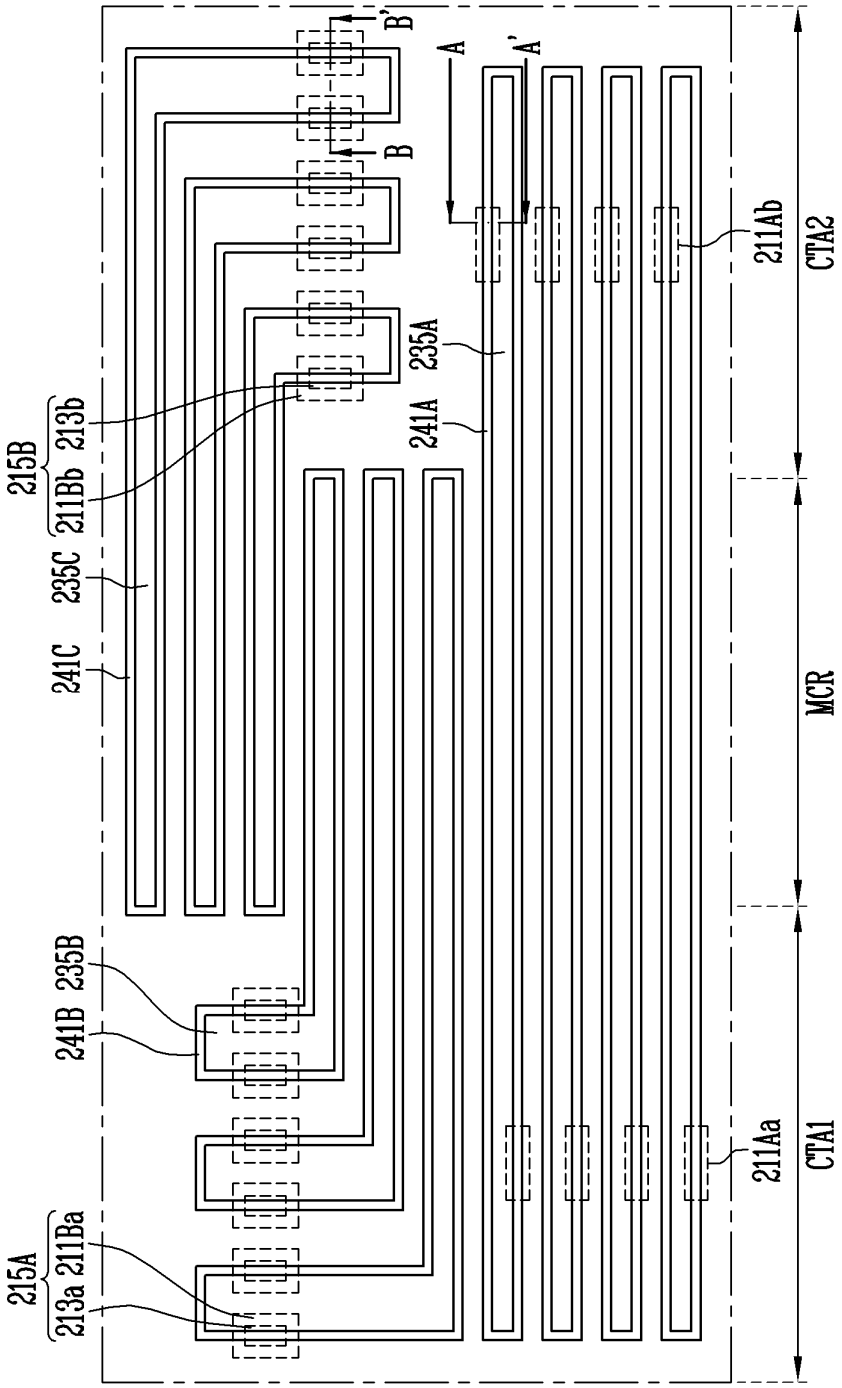

B'
B
A
A'
211Ab
CTA2
235A
241A
215B
213b
211Bb
235C
241C
MCR
235B
241B
215A
211Ba
213a
211Aa
CTA1

FIG. 12B

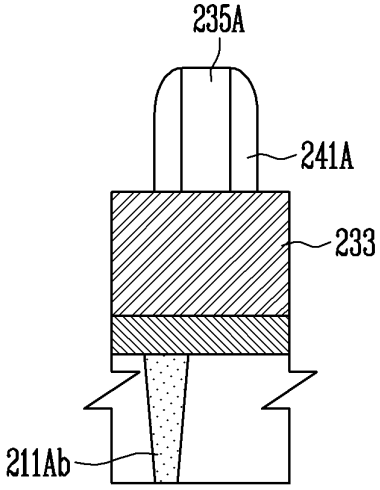


FIG. 12C

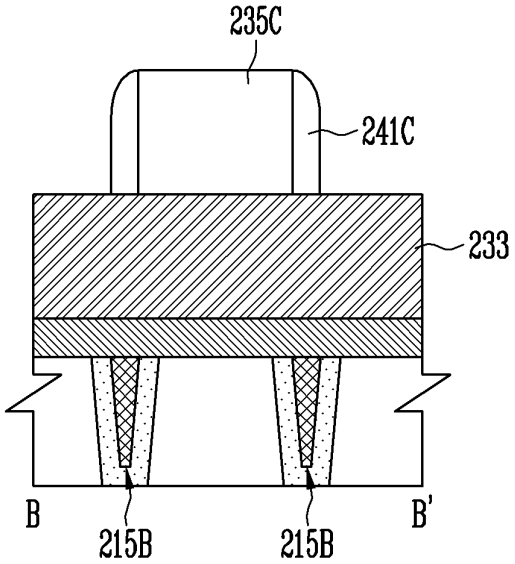


FIG. 13

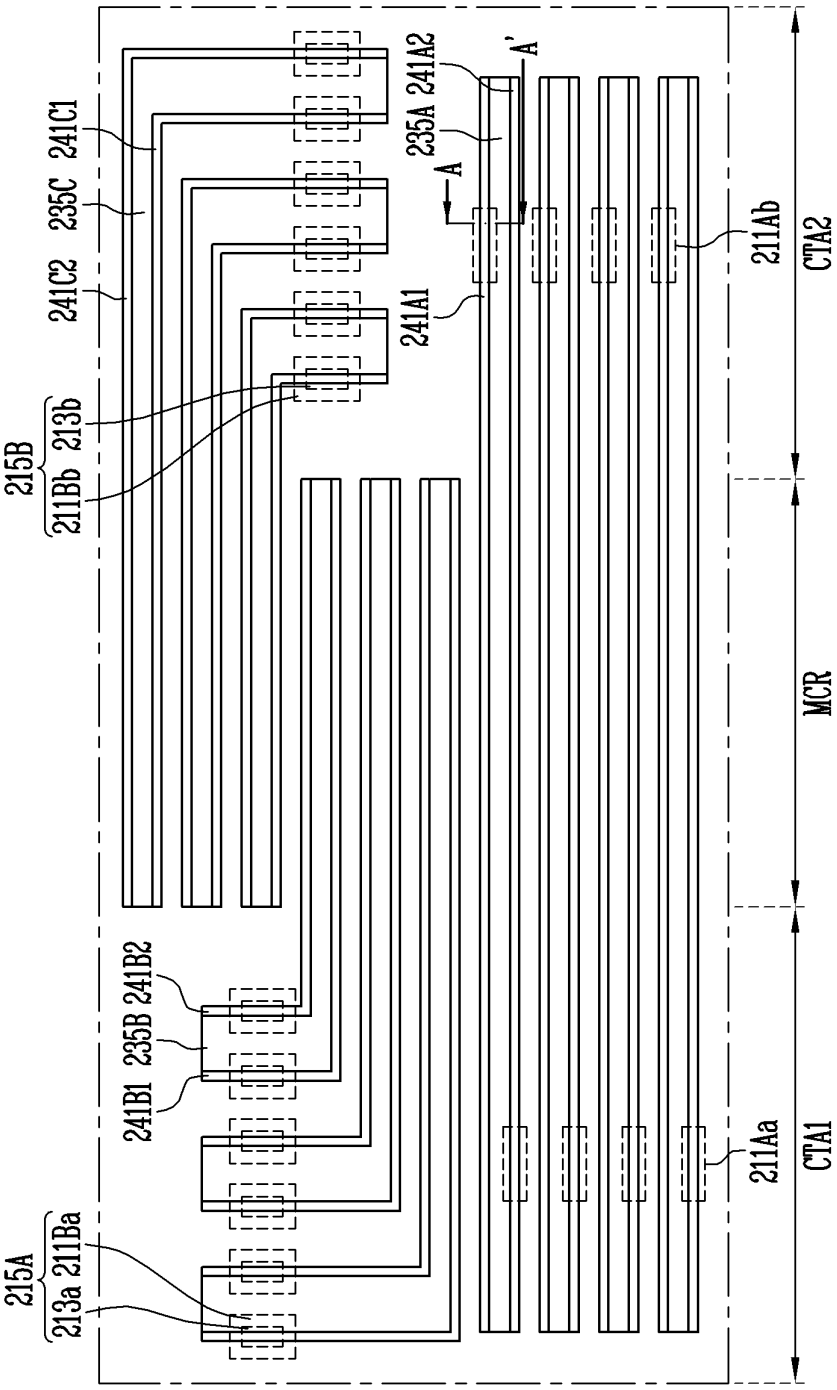

241C1
235C
241C2
215B
213b
211Bb
241B2
235B
241B1
215A
211Ba
213a
241A2
235A
A
A'
241A1
211Ab
CTA2
MCR
211Aa
CTA1

FIG. 14A

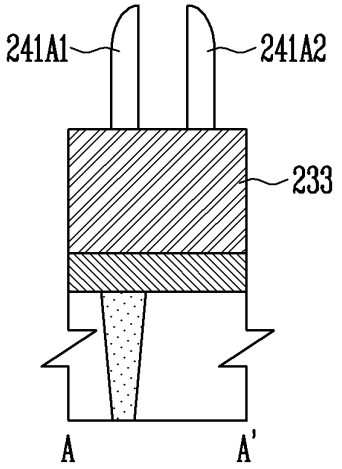


FIG. 14B

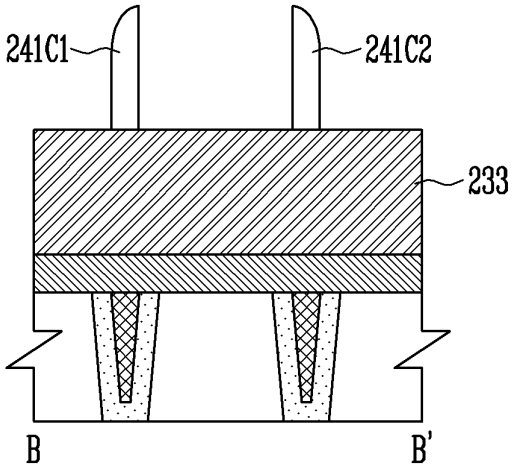


FIG. 15A

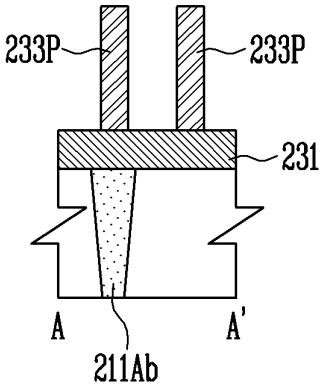


FIG. 15B

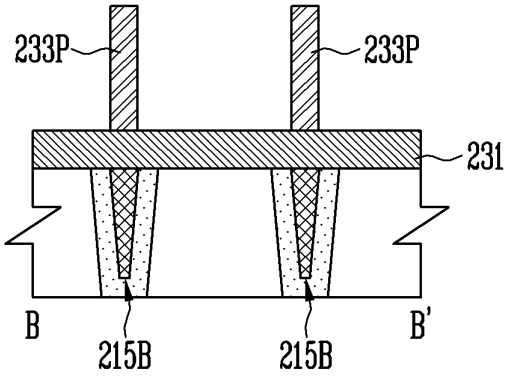


FIG. 16A

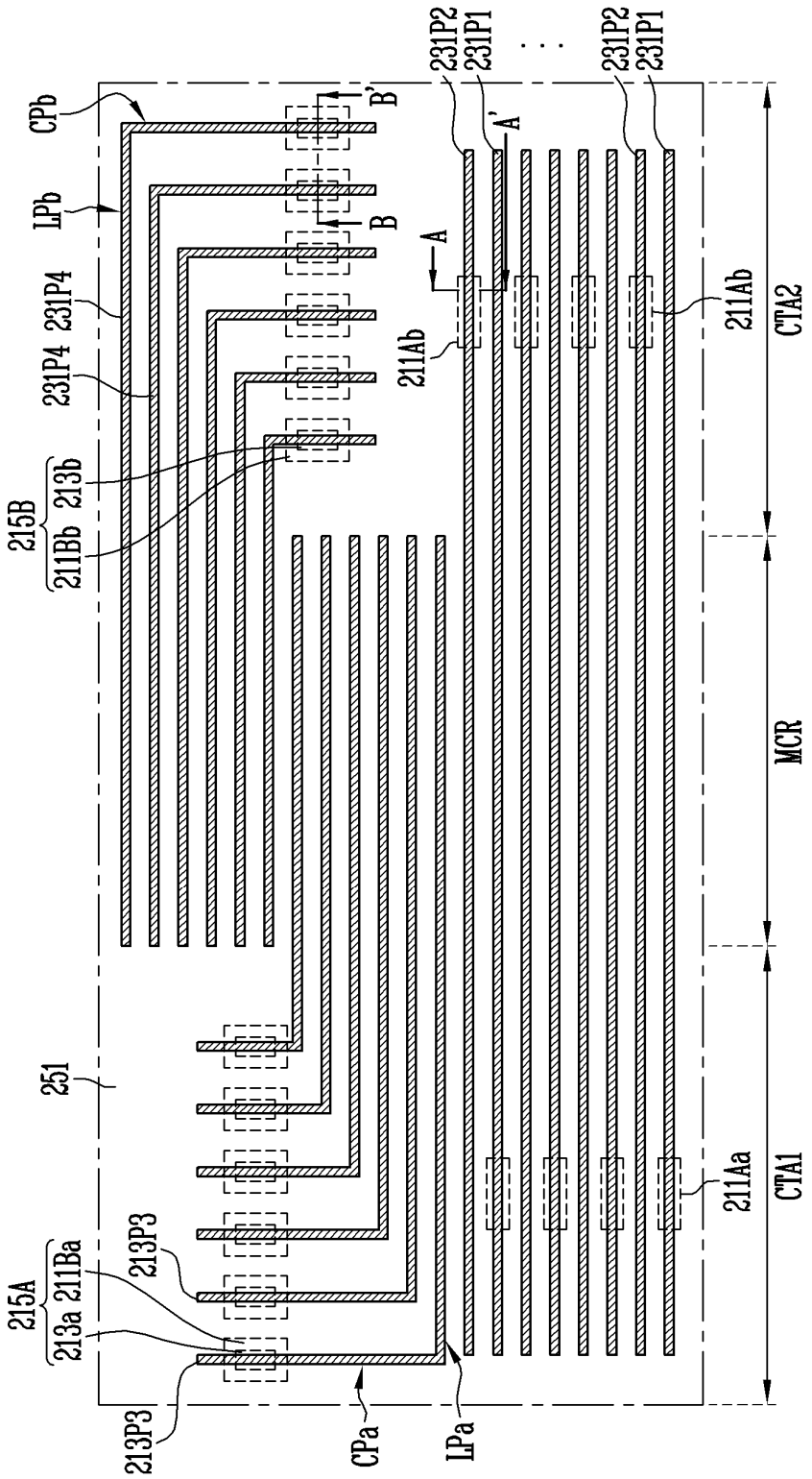

CPb
LPb
231P4
231P4
215B
213b
211Bb
251
215A
211Ba
213a
213P3
213P3
CPa
LPa
B
B'
A
A'
231P2
231P1
231P2
231P1
211Ab
211Ab
211Aa
CTA2
MCR
CTA1

FIG. 16B

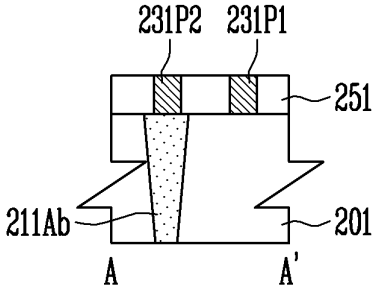


FIG. 16C

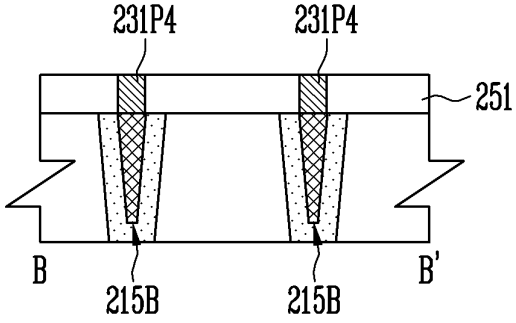


FIG. 17

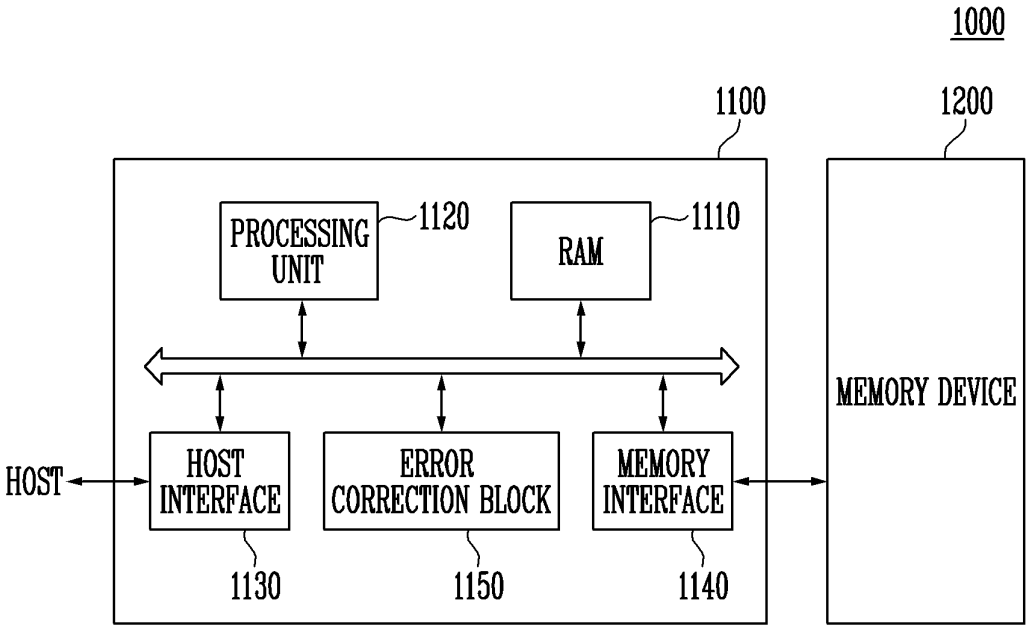

1000
1100
1200
PROCESSING UNIT
1120
RAM
1110
MEMORY DEVICE
HOST
HOST INTERFACE
ERROR CORRECTION BLOCK
MEMORY INTERFACE
1130
1150
1140

FIG. 18

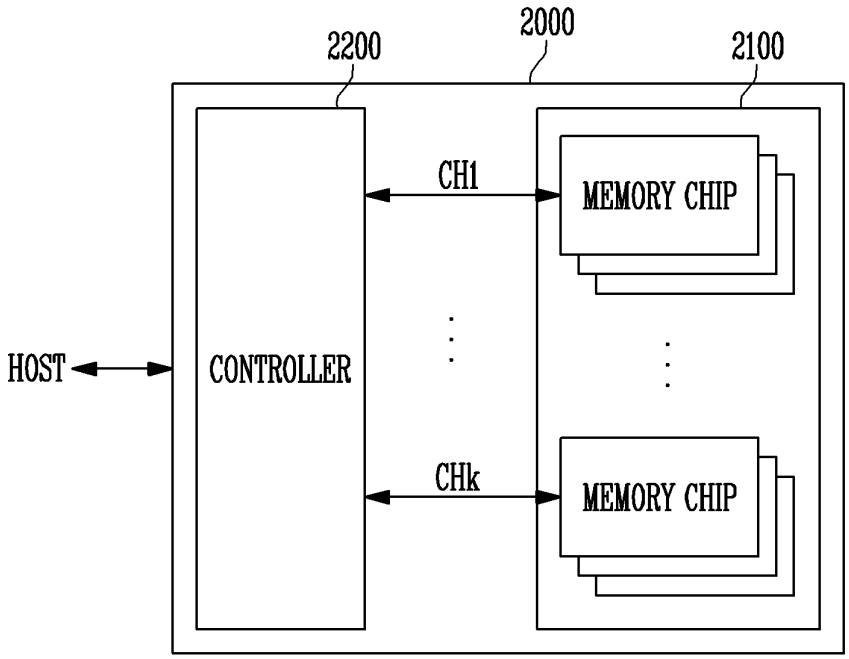
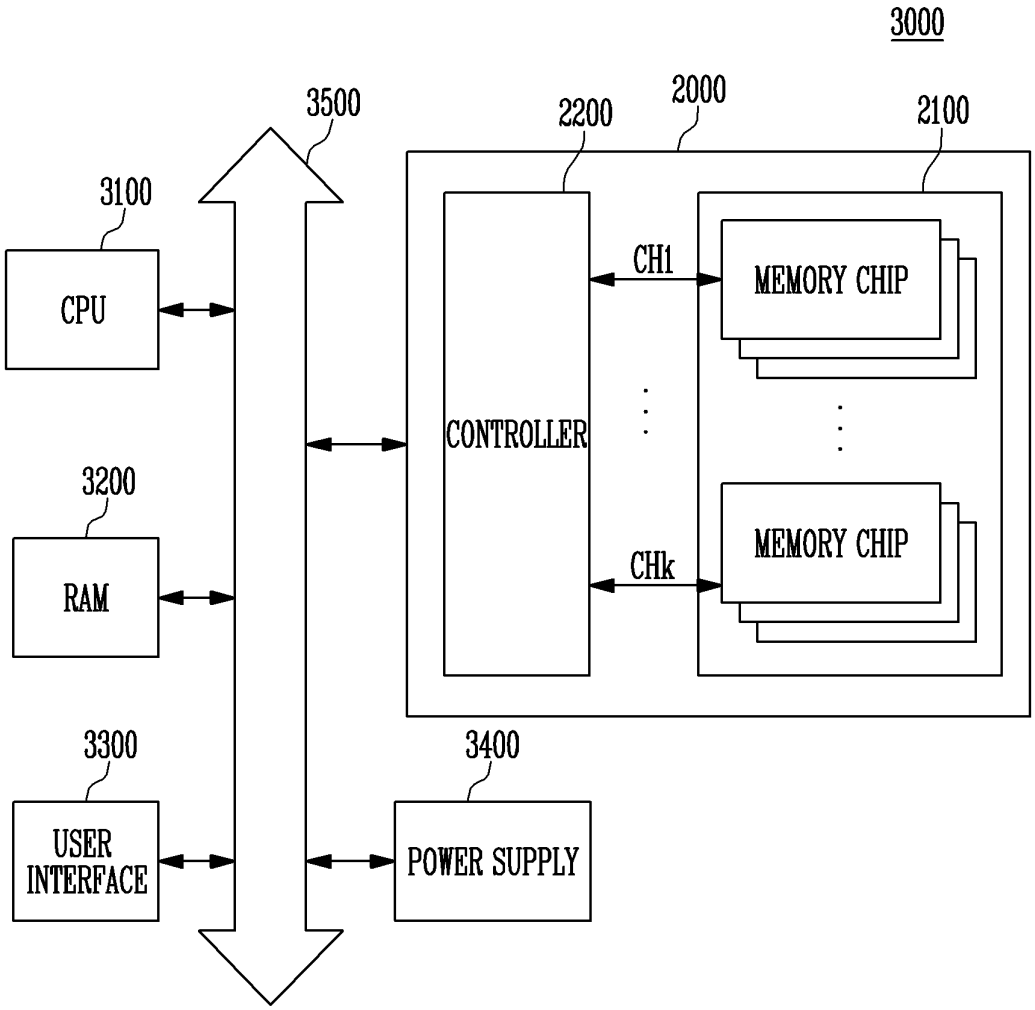

2200
2000
2100
CH1
MEMORY CHIP
HOST
CONTROLLER
CHk
MEMORY CHIP

FIG. 19


3000
3500
2200
2000
2100
3100
CPU
CH1
MEMORY CHIP
CONTROLLER
3200
RAM
CHk
MEMORY CHIP
3300
3400
USER INTERFACE
POWER SUPPLY