Fig. 1

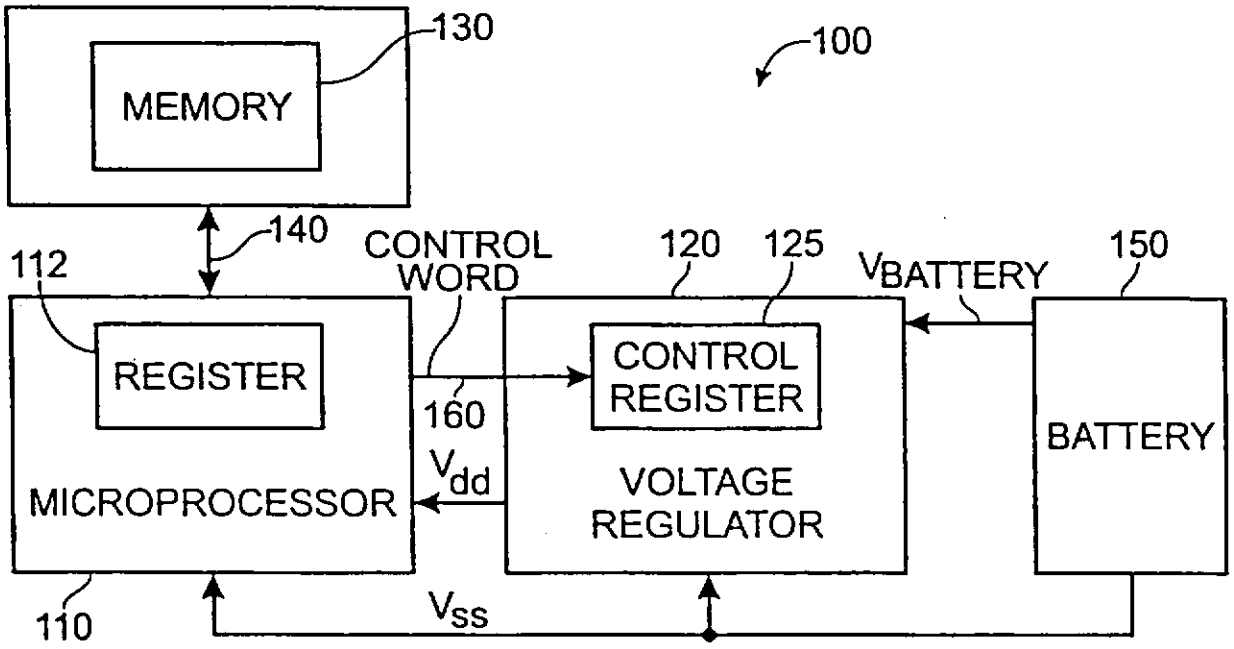

MEMORY
130
100
140
CONTROL WORD
120
125
VBATTERY
150
112
REGISTER
160
CONTROL REGISTER
BATTERY
Vdd
MICROPROCESSOR
VOLTAGE REGULATOR
110
Vss

Fig. 2

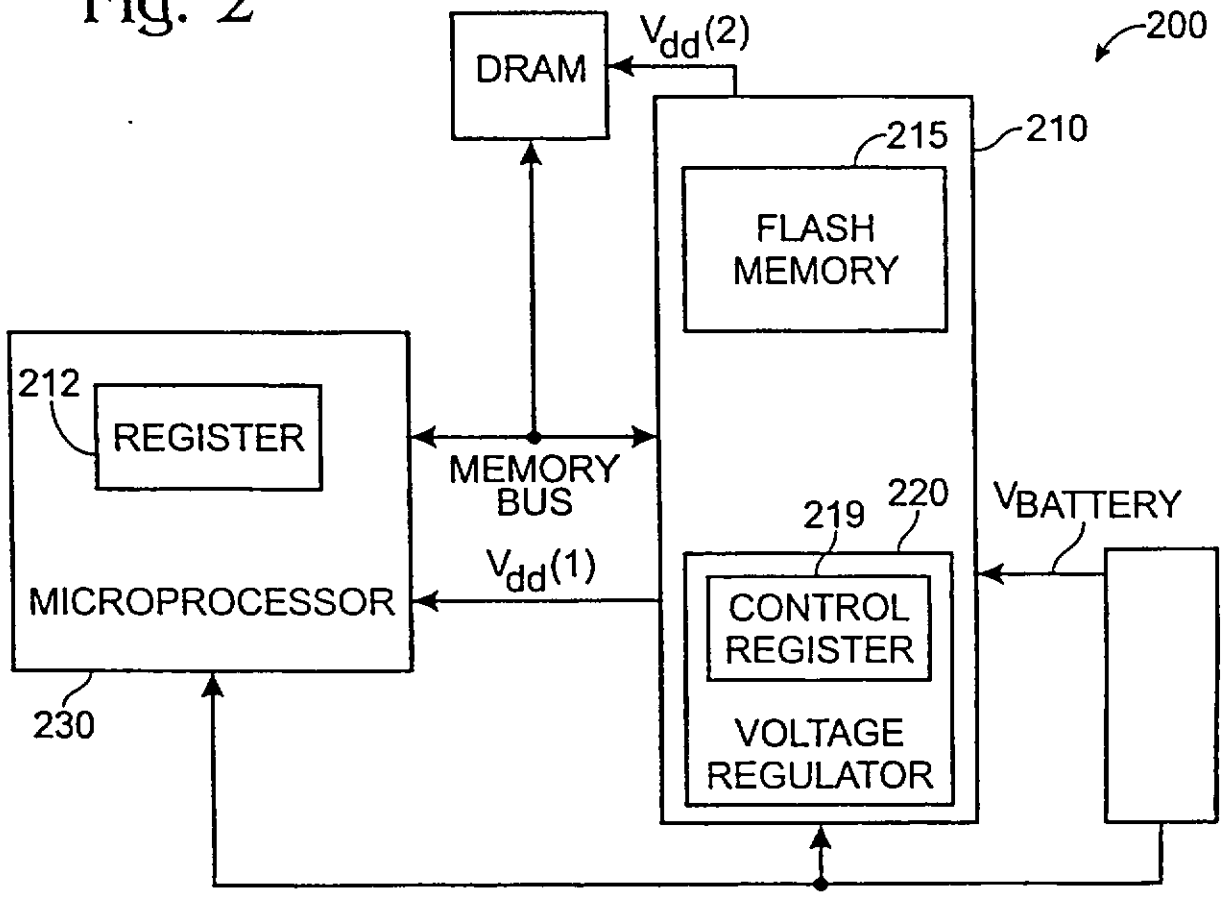

DRAM
Vdd(2)
200
215
210
FLASH MEMORY
212
REGISTER
MEMORY BUS
219
220
VBATTERY
Vdd(1)
CONTROL REGISTER
MICROPROCESSOR
VOLTAGE REGULATOR
230

Fig. 3

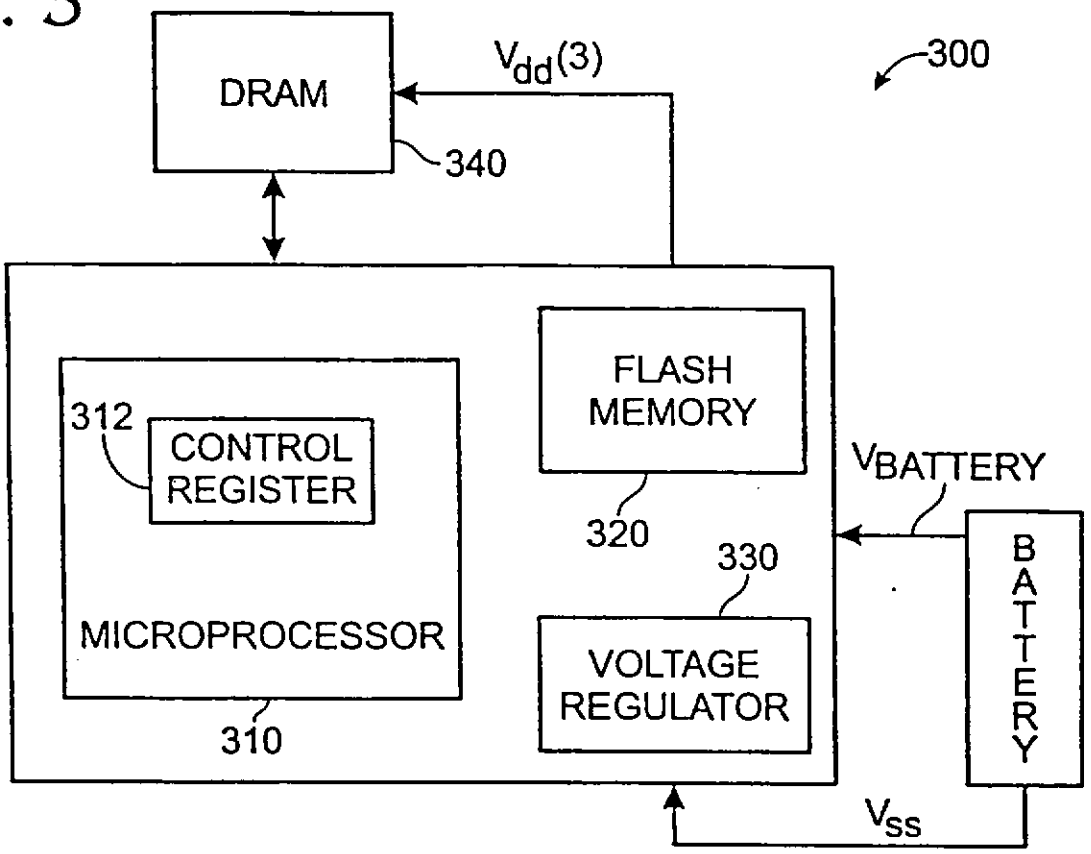

DRAM
$V_{dd}(3)$
300
340
FLASH MEMORY
312
CONTROL REGISTER
320
330
$V_{BATTERY}$
MICROPROCESSOR
VOLTAGE REGULATOR
BATTERY
310
V_{ss}

Fig. 4

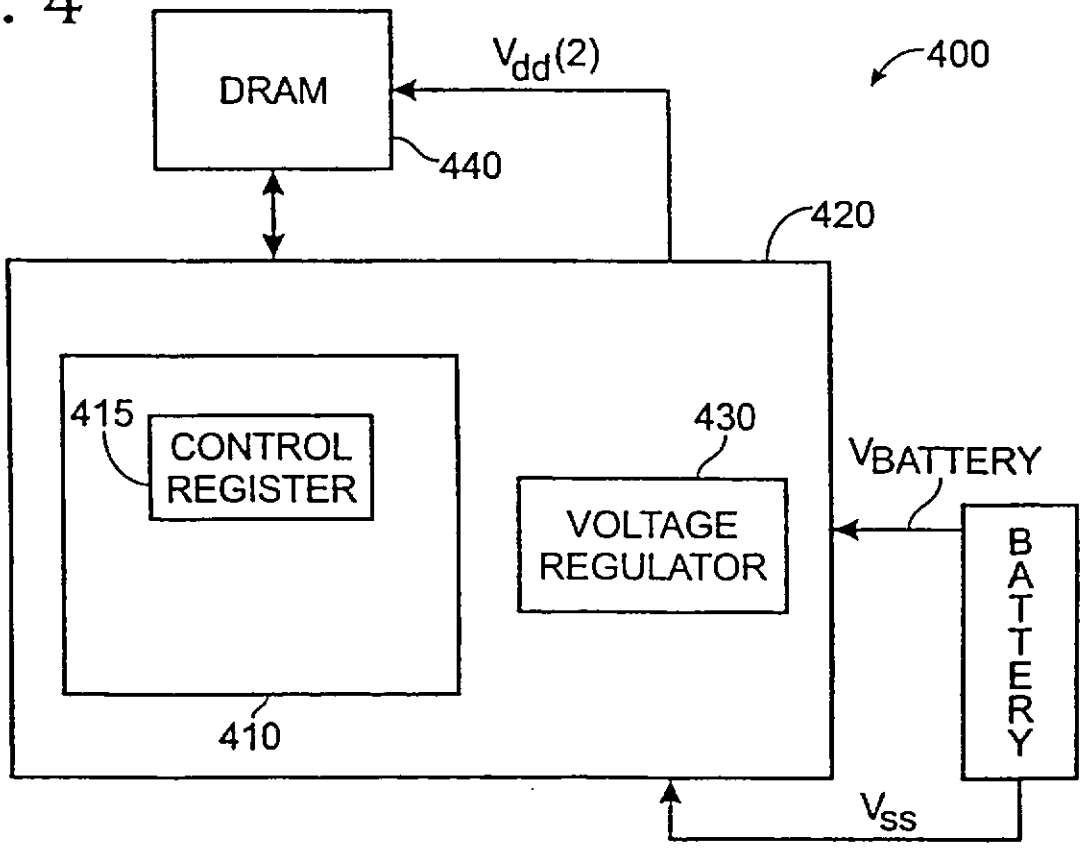

DRAM
$V_{dd}(2)$
400
440
420
415
CONTROL REGISTER
430
$V_{BATTERY}$
VOLTAGE REGULATOR
BATTERY
410
V_{ss}

Fig. 5

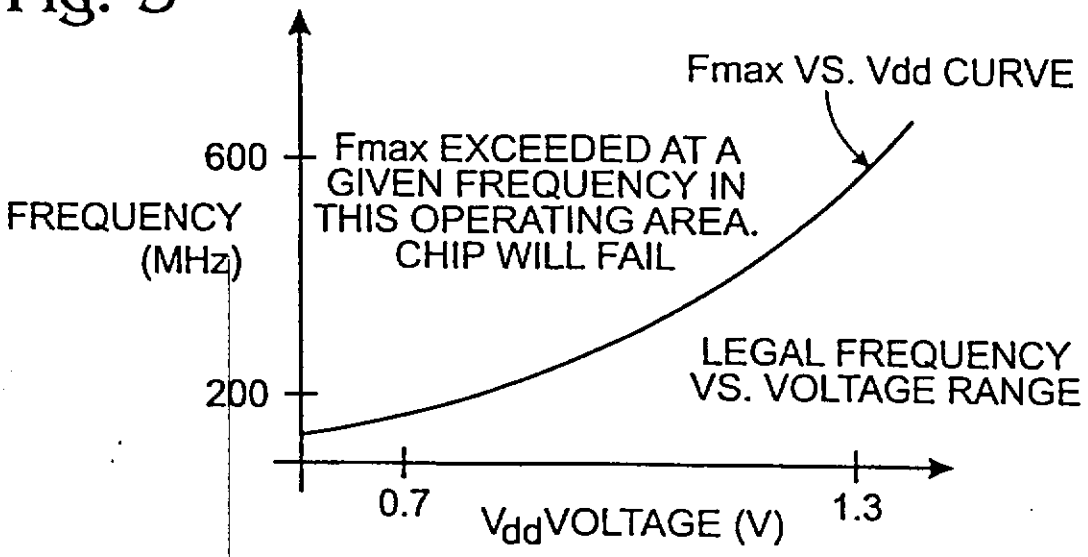


Fig. 6

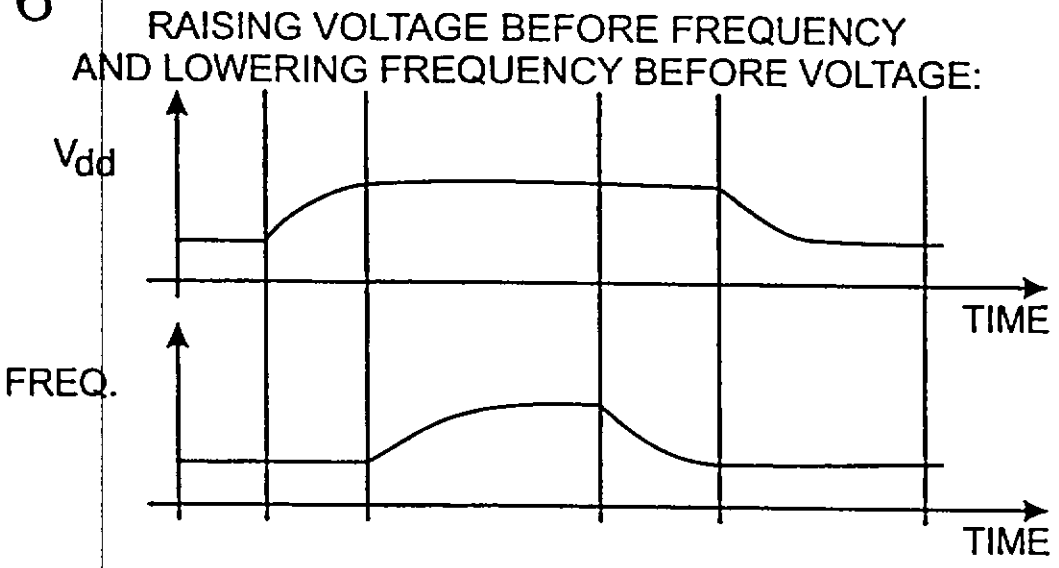
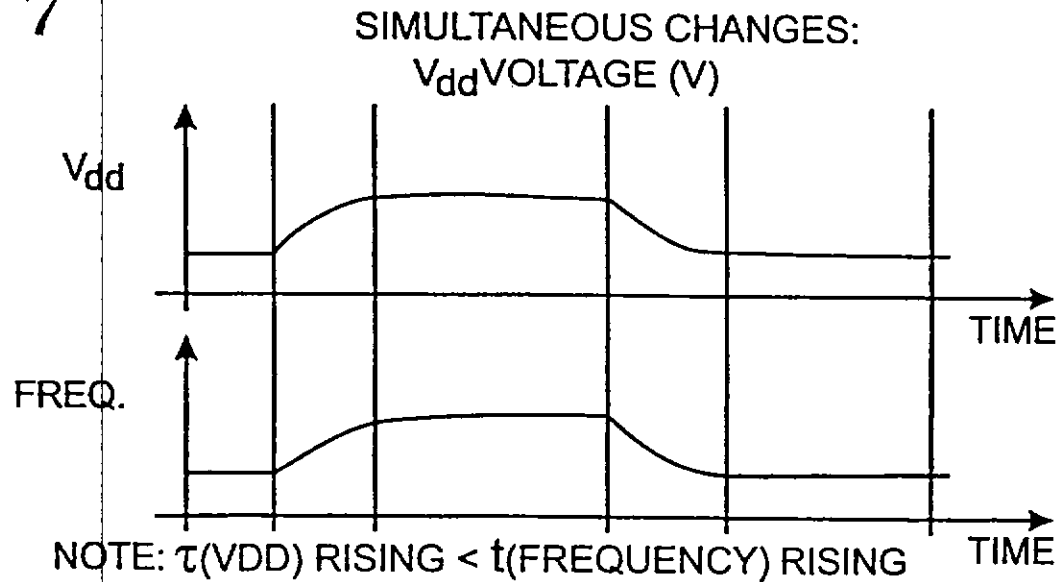


Fig. 7



NOTE: τ(VDD) RISING < t(FREQUENCY) RISING
τ(VDD) FALLING > t(FREQUENCY) FALLING