

ABSTRACT

POWER LDMOS TRANSISTOR

An LDMOS device comprises a substrate having a first conductivity type and a lightly doped epitaxial layer thereon having an upper surface. Source and drain regions of the first conductivity type are formed in the epitaxial layer along with a channel region of a second conductivity type formed therebetween. A conductive gate is formed over a gate dielectric layer. A drain contact electrically connects the drain region to the substrate, comprising a first trench formed from the upper surface of the epitaxial layer to the substrate and having a side wall along the epitaxial layer, a highly doped region of the first conductivity type formed along the side wall of the first trench, and a drain plug in the first trench adjacent the highly doped region. A source contact is provided and an insulating layer is formed between the conductive gate and the source contact.

[Figure 1]