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ABSTRACT

The invention relates to a signal processing apparatus comprising plural memories in an LSI and plural memory access blocks for accessing these memories, in which the cause can be analyzed easily in the event of a fault.

The signal processing apparatus 100 comprises a first arbitration block 150 for arbitrating the access right of a third memory access block 130 to a first built-in memory 160, a second arbitration block 180 for arbitrating to store the memory access history of the third memory access block 130 in a second built-in memory 190 which is not the same memory as the first built-in memory 160 executing the access of the third memory access block 130, and a trace control block 170 for controlling.