

ABSTRACT

A delay circuit (10) contains a first inversion circuit including a pull-up circuit (2) and a pull-down circuit (3), and a second inversion circuit including a pull-up circuit (4) and a pull-down circuit (5). The delay circuit further contains a first pass transistor (6) connected in series to the pull-up circuit in the first inversion circuit between a power supply potential and an output node (Out), a second pass transistor (7) connected in series to the pull-down circuit in the first inversion circuit between a ground potential and the output node, a third pass transistor (8) connected in series between the input node (In) and the pull-up circuit in the second inversion circuit, and a fourth pass transistor (9) connected in series between the input node and the pull-down circuit in the second inversion circuit. A delay characteristic of the delay circuit is changed by a combination of control signals (C1 to C4) applied to gates of the first to fourth pass transistors.