Claims

What is claimed is

1. A method for synchronizing video output towards a single display frequency comprising:

    - providing a shared reference signal for synchronizing, at the single display frequency, video output between two or more image generator processors each driving at least one independent video card, wherein each of the independent video cards supports on-the-fly image refresh rate adaptation based on responsiveness from the corresponding image generator processor; and

    - at each one of the image generator processors, artificially affecting, in real-time, image generation rendering speed during a next frame generation processing to trigger the on-the-fly image refresh rate adaptation by the one image generator processor's video card for proactively scheduling refresh of an image corresponding to the next frame by the one image generator processor's video card, thereby aligning the refresh of the image to the shared reference signal while avoiding manipulation of memory registers of the one image generator processor's video card by the one image generator processor.

2. The method for synchronizing video output of claim 1, wherein artificially affecting, in real-time, image generation rendering speed is performed by programmatically mimicking, in real-time, image generation rendering lag during the next frame generation processing.

3. The method for synchronizing video output of claim 1 or claim 2, wherein artificially affecting, in real-time, image generation rendering speed is performed by programmatically mimicking, in real-time, image generation rendering hastening during the next frame generation processing.

4. The method for synchronizing video output of claim 1, wherein, when the one image generator processor is a master image generator processor, artificially affecting, in real-time, image generation rendering speed involves scheduling the next frame generation processing by a predetermined target timer linked to the shared reference signal while avoiding manipulation of the video card's memory registers by the master image generator processor.

5. The method for synchronizing video output of claim 1 or claim 4, wherein, when the one image generator processor is a slave image generator processor and unless the shared reference signal is aligned to a local slave signal, artificially affecting, in real-time, image generation rendering speed involves scheduling the next frame generation processing by varying a mimicked rendering timer in real-time during a next slave frame processing to trigger the on-the-fly image refresh rate adaptation by the slave image generator processor's video card for reducing a time distance between the shared reference and the local slave signal, thereby improving synchronicity of an image corresponding to the next slave frame and an image corresponding to another next frame from another of the two or more image generator processors while avoiding manipulation of the video card's memory registers by the slave image generator processor.

6. The method for synchronizing video output of claim 5, further comprising sending, from the slave image generator processor towards a reference signal generator, an indication of the time distance between the slave local signal and the shared reference signal.

7. The method for synchronizing video output of claim 6, wherein the indication comprises the time distance between the shared reference and the local slave reference signal.

8. The method for synchronizing video output of claim 6 or claim 7, wherein the reference signal generator is provided by a master image generator processor from the two or more image generator processors.

9. The method for synchronizing video output of any one of claims 6 to 8, further comprising updating the shared reference signal by adjusting the predetermined target timer at the reference signal generator considering a plurality of received indications comprising the received indication of the time distance between the slave local signal and the shared reference signal.

10. The method for synchronizing video output of claim 9, wherein adjusting the predetermined target timer is performed by subtracting a minimum value from a plurality of received time distances from the plurality of received indications.

11. The method for synchronizing video output of any one of claims 5 to 10, wherein when the one image generator processor is the slave image generator processor and when the shared reference signal is aligned with the local slave reference signal, processing the next frame without modifying the mimicked rendering timer.

12. The method of claim 2 further comprising, independently from each of the two or more image generator processors, providing each of the images corresponding to each of the next frame at the single display frequency.

13. A system comprising:

- a display system for displaying a synchronized composite image thereon at a single display frequency;

- a plurality of independent video cards each configured for supporting on-the-fly image refresh rate adaptation based on responsiveness from a corresponding image generator process; and

- a plurality of image generator processors each configured for driving one or more of the plurality of independent video cards and having access to a shared reference signal;

- wherein each one of the plurality of image generator processors is configured for artificially affecting, in real-time, image generation rendering speed during a next frame generation processing to trigger the on-the-fly image refresh rate adaptation by the one image generator processor's video card for proactively scheduling refresh of an image corresponding to the next frame by the one image generator processor's video card, thereby aligning the refresh of the image to the shared reference signal while avoiding manipulation of memory registers of the one image generator processor's video card by the one image generator processor;

- wherein the composite image comprises each of the images corresponding to the next frames from each one of the plurality of image generator processors.

14. The system of claim 13, wherein the one image generator processor is configured for artificially affecting, in real-time, image generation rendering speed by programmatically mimicking, in real-time, image generation rendering lag during the next frame generation processing.

15. The system of claim 13, wherein the one image generator processor is configured for artificially affecting, in real-time, image generation rendering speed by programmatically mimicking, in real-time, image generation rendering hastening during the next frame generation processing.

16. The system of claim 13, wherein the plurality of image generator processors comprise a master mage generator processor and one or more slave image generator processor and, when the one image generator processor is the master image generator processor, the master image generator processor is configured for artificially affecting, in real-time, image generation rendering speed during the next frame generation processing by scheduling a next master frame generation processing by a predetermined target timer linked to the shared reference signal while avoiding manipulation of the video card's memory registers by the master image generator processor.

17. The system of claim 13, wherein the plurality of image generator processors comprise one or more slave image generator processor and, when the one image generator processor is the slave image generator processor and unless the shared reference signal is aligned to a local slave signal, the slave image generator processor is configured for artificially affecting, in real-time, image generation rendering speed during the next frame generation processing by varying a mimicked rendering timer in real-time during a next slave frame processing to trigger the on-the-fly image refresh rate adaptation by the slave image generator processor's video card for reducing a time distance between the shared reference and the local slave signal, thereby improving synchronicity of an image corresponding to the next slave frame and an image corresponding to another next frame from another of the plurality of image generator processors while avoiding manipulation of the video card's memory registers by the slave image generator processor.

18. The system of claim 17, wherein the slave image generator processor is further configured for sending, towards a reference signal generator, an indication of the time distance between the slave local signal and the shared reference signal.

19. The system of claim 18, wherein the indication comprises the time distance between the shared reference and the local slave reference signal.

20. The system of claim 18, wherein the reference signal generator is configured to update the shared reference signal by adjusting the predetermined target timer considering a plurality of received indications comprising the received indication of the time distance between the slave local signal and the shared reference signal.