

What is claimed is:

1. A nonvolatile memory device comprising:

a memory cell array comprising a plurality of memory blocks, each of the plurality of memory blocks comprising a plurality of memory cells coupled to word-lines respectively, the word-lines being stacked vertically on a substrate, some memory cells of the plurality of memory cells being selectable by a sub-block unit smaller than one memory block of the plurality of memory blocks; and

a control circuit configured to divide sub-blocks of a first memory block of the plurality of memory blocks into at least one bad sub-block and at least one normal sub-block based on error occurrence frequency of each of the sub-blocks of the first memory block, and configured to apply different program/erase cycles to the at least one bad sub-block than to the at least one normal sub-block based on a command and an address provided from external to the nonvolatile memory device,

wherein the at least one bad sub-block is adjacent the at least one normal sub-block.

2. The nonvolatile memory device of claim 1,

wherein the control circuit is further configured to apply a first program/erase cycle to the at least one normal sub-block when the address designates the at least one normal sub-block, and apply a second program/erase cycle to the at least one bad sub-block when the address designates the at least one bad sub-block, and

wherein the second program/erase cycle runs in a second time interval that is less than a first time interval of the first program/erase cycle.

3. The nonvolatile memory device of claim 1,

wherein the control circuit is further configured to apply a first program/erase cycle to the at least one normal sub-block when the address designates the at least one normal sub-block, and apply a second program/erase cycle to the at least one bad sub-block until a first reference cycle value and apply a third program/erase cycle to the at least one bad sub-block after the first reference cycle value when the address designates the at least one bad sub-block; and

wherein the second program/erase cycle runs in a first time interval that is less than a second time interval of the first program/erase cycle, and

wherein the third program/erase cycle runs in a third time interval that is less than the second time interval of the second program/erase cycle.

4. The nonvolatile memory device of any one of claims 1 to 3, further comprising:

a voltage generator configured to generate word-line voltages based on control signals; and

an address decoder configured to transfer the word-line voltages to the at least one bad sub-block and the at least one normal sub-block in response to a row address of the address,

wherein the control circuit is further configured to control the voltage generator and the address decoder in response to the command and the address.

5. The nonvolatile memory device of claim 4, wherein the control circuit comprises:

a bad sub-block information register configured to store bad row addresses of word-lines included in the at least one bad sub-block;

a command decoder configured to decode the command to provide a decoded command;

an address comparator configured to compare the row address with each of the bad row addresses to output a match signal indicating a result of the comparison;

a program/erase cycle information register configured to store program/erase cycle information associated with a first program/erase cycle applied to the at least one normal sub-block and a second program/erase cycle applied to the at least one bad sub-block; and

a control signal generator configured to generate the control signals and a first mode signal and a second mode signal that control the address decoder in response to the decoded command and the match signal and based on the program/erase cycle information register.

6. The nonvolatile memory device of claim 4, wherein the control circuit comprises:

a bad sub-block information register configured to store bad row addresses of word-lines included in the at least one bad sub-block;

a command decoder configured to decode the command to provide a decoded command;

an address comparator configured to compare the row address with each of the bad row addresses to output a match signal indicating a result of the compare;

a program/erase cycle counter configured to count a number of program/erase cycles on the at least one bad sub-block to output a counting value, in response to the decoded command and the match signal;

a comparator configured to compare the counting value with a reference counting value to generate a comparison signal;

a program/erase cycle information register configured to store program/erase cycle information associated with a first program/erase cycle applied to the at least one normal sub-block and a second program/erase cycle applied to the at least one bad sub-block; and

a control signal generator configured to generate the control signals and a first mode signal and a second mode signal that control the address decoder in response to the decoded command and the match signal and based on the program/erase cycle information register.

7. The nonvolatile memory device of any one of claims 4 to 6, wherein, when the command is an erase command to the first memory block, and

wherein the control circuit is further configured to control the voltage generator and the address decoder such that an erase bias condition is different during an erase operation on the first memory block based on whether the at least one bad sub-block is programmed.

8. The nonvolatile memory device of claim 7,

wherein, when the at least one bad sub-block is not programmed, the control circuit is further configured to control the address decoder to apply an erase voltage to the substrate, apply a first word-line erase voltage to word-lines associated with the at least one normal sub-block, and apply a second word-line erase voltage to word-lines associated with the at least one bad sub-block, and

wherein a level of the second word-line erase voltage is higher than a level of the first word-line erase voltage.

9. The nonvolatile memory device of claim 7, wherein, when the at least one bad

sub-block is programmed, the control circuit is further configured to control the address decoder to maintain a level of an erase voltage applied to the substrate at a first level during a first time interval and to maintain the level of the erase voltage at a second level that is higher than the first level during a second time interval succeeding to the first time interval such that the at least one bad sub-block is erased prior to the at least one normal sub-block.

10. The nonvolatile memory device of any one of claims 4 to 6, wherein, when the command is a read command to the at least one normal sub-block, the control circuit is further configured to control the voltage generator and the address decoder such that a read bias condition is different during a read operation on the at least one normal sub-block, based on whether the at least one bad sub-block is programmed.

11. The nonvolatile memory device of any one of claims 4 to 10,
wherein each of the memory cells is configured to store M-bits, M being an integer greater than one, and

wherein ones of the memory cells coupled to a boundary word-line of word-lines of the at least one normal sub-block is configured to store N-bits, the boundary word-line being adjacent to the at least one bad sub block, and N being a natural number smaller than M.

12. The nonvolatile memory device of any one of claims 1 to 11, wherein a number of word-lines included in the at least one bad sub-block varies according to a position at which the first memory block is formed in the memory cell array.

13. A method of operating a nonvolatile memory device, wherein the nonvolatile memory device comprises a memory cell array comprising a plurality of memory blocks, each of the plurality of memory blocks comprising a plurality of memory cells coupled to word-lines respectively, the word-lines being stacked vertically on a substrate, some memory cells of the plurality of memory cells being selected by a sub-block unit that is smaller than one memory block, the method comprising:

dividing sub-blocks of a first memory block of the plurality of memory blocks into at least one bad sub-block and at least one normal sub-block based on error occurrence frequency of each of the sub-blocks of the first memory block, the at least one bad

sub-block and the at least one normal sub-block being adjacent to each other; and

applying different program/erase cycles to the at least one bad sub-block and the at least one normal sub-block based on a command and an address provided from external to the nonvolatile memory device.

14. The method of claim 13, wherein applying the different program/erase cycles comprises:

determining whether the address designates the at least one bad sub-block;

performing a first program/erase cycle on the at least one normal sub-block, when the address designates the at least one normal sub-block; and

performing a second program/erase cycle on the at least one bad sub-block, when the address designates the at least one bad sub-block.

15. The method of claim 13 or claim 14, further comprising:

adjusting a bias condition applied to the first memory block based on whether the at least one bad sub-block is programmed during a memory operation in the first memory block; and

performing the memory operation on the first memory block according to the adjusting the bias condition.

16. The method of claim 15, wherein the memory operation is a read operation on the at least one normal sub-block, and wherein adjusting the bias condition comprises:

applying a first read pass voltage to unselected word-lines in the at least one normal sub-block when the at least one bad sub-block is not programmed; and

applying a second read pass voltage to the unselected word-lines in the at least one normal sub-block when the at least one bad sub-block is programmed,

wherein a level of the second read pass voltage is higher than a level of the first read pass voltage.

17. The method of claim 15 or claim 16, wherein the memory operation comprises an erase operation on the first memory block when the at least one bad sub-block is not programmed, wherein adjusting the bias condition comprises:

applying an erase voltage to the substrate;

applying a first word-line erase voltage to word-lines of the at least one normal sub-block; and

applying a second word-line erase voltage to word-lines of the at least one bad sub-block,

wherein a level of the second word-line erase voltage is higher than a level of the first word-line erase voltage.

18. The method of claim 15 or claim 16, wherein the memory operation is an erase operation on the first memory block when the at least one bad sub-block is programmed, wherein adjusting the bias condition comprises:

maintaining an erase voltage applied to the substrate at a first level during a first time interval; and

maintaining the erase voltage applied to the substrate at a second level during a second time interval succeeding to the first time interval,

wherein the second level is higher than the first level.

19. A storage device comprising:

at least one nonvolatile memory device; and

a memory controller configured to control the at least one nonvolatile memory device,

wherein the at least one nonvolatile memory device comprises:

a memory cell array comprising a plurality of memory blocks, each of the plurality of memory blocks comprising a plurality of memory cells coupled to word-lines respectively, the word-lines being stacked vertically on a substrate, some memory cells of the plurality of memory cells being selected by sub-block unit smaller than one memory block of the plurality of memory blocks; and

a control circuit configured to control access on the memory cell array based on a command and an address provided from the memory controller,

wherein the memory controller is configured to transmit, to the at least one nonvolatile memory device, bad sub-block information associated with bad sub-block included in each of the memory blocks,

wherein the control circuit is configured to divide sub-blocks of a first memory block of the plurality of memory blocks into at least one bad sub-block and at least one

normal sub-block based on error occurrence frequency of each of the sub-blocks of the first memory block, and configured to apply different program/erase cycles to the at least one bad sub-block and the at least one normal sub-block based on the command and the address provided from the memory controller to the nonvolatile memory device, and further configured to apply different bias conditions to the at least one bad sub-block and the at least one normal sub-block during a memory operation on the first memory block, and

wherein the at least one bad sub-block and the at least one normal sub-block are adjacent each other.

20. The storage device of claim 19, wherein the memory controller comprises an error correction code (ECC) engine configured to perform error detection and correction on data read from the at least one nonvolatile memory device and is configured to generate the bad sub-block information.