CLAIMS

We claim:

1. An **apparatus** for reducing switching jitter, comprising:

a pattern dependent delay circuit including:

a pattern detector to detect a switching pattern of at least three data signals on respective wires; and

a delay module coupled to the pattern detector to adaptively change delays of the at least three data signals based on the detected switching pattern; and

a transmitter, coupled to the pattern dependent delay circuit, to transmit the at least three data signals.

2. The apparatus of claim 1, wherein individual data signals of the at least three data signals switch between at least three logic states.

3. The apparatus of claim 2, wherein the at least three data signals are in different logic states.

4. The apparatus of any one of claims 1-3, wherein the pattern detector is to detect the switching pattern based on a prior logic state and a current logic state of the at least three data signals.

5. The apparatus of claim 1, wherein the pattern detector is to send one or more control signals to the delay module to change the delays of the at least three data signals when the pattern detector detects that the at least three data signals are each undergoing a state transition during a same time period.

6. The apparatus of claim 1, wherein the delay module is to cause different delays for each of the at least three data signals.

7. The apparatus of claim 1, wherein the delay module comprises a plurality of delay controllers and a plurality of samplers, wherein individual delay

controllers are paired with individual samplers to cause delay of respective individual data signals of the at least three data signals.

8. The apparatus of claim 1, wherein the pattern dependent delay circuit is to adaptively change the delays of the at least three data signals before the transmitter transmits the at least three data signals to reduce a switching jitter associated with the at least three data signals.

9. The apparatus of claim 1, wherein the pattern dependent delay circuit is to reduce a channel physical layer (C-PHY) switching jitter.

10. The apparatus of claim 1, wherein the transmitter is a mobile industry processor interface (MIPI) channel physical layer (C-PHY) compliant transmitter.

11. A **system** for reducing switching jitter, comprising:

a processor;

a controller coupled to the processor to output data processed by the processor;

a transmitter coupled to the controller to transmit the data using at least three data signals, wherein individual data signals of the at least three data signals switch between at least three logic states; and

a pattern dependent delay circuit, coupled to the transmitter, to detect a switching pattern of the at least three data signals and adaptively reduce a switching jitter based on the detected switching pattern.

12. The system of claim 11, wherein the pattern dependent delay circuit is to reduce a channel physical layer (C-PHY) switching jitter by changing delays on the at least three data signals before the transmitter transmits the at least three data signals.

13. The system of claim 11 or 12, wherein the transmitter is a MIPI® channel physical layer (C-PHY) compliant transmitter.

14. A **method** for reducing switching jitter, comprising:

detecting a switching pattern of a plurality of data signals on respective wires;

causing a delay on one or more of the plurality of data signals based on the detected switching pattern; and

transmitting the plurality of data signals.

15. The method of claim 14, wherein the detecting comprises detecting a logic state of individual data signals of the plurality of data signals, wherein the logic state is one of at least three possible logic states.

16. The method of claim 14 or 15, wherein the detecting comprises detecting the switching pattern based on a prior logic state and a current logic state of the plurality of data signals.

17. The method of claim 14 or 15, wherein the causing the delay is responsive to a detection that each of the plurality of data signals switches to a different logic state from a prior logic state.

18. The method of claim 14, wherein the causing comprises changing delays on each of the plurality of data signals based on the switching pattern.

19. The method of claim 14, wherein the causing comprises causing different delays on each of the plurality of data signals based on the switching pattern.

20. The method of claim 14, wherein the causing comprises reducing a channel physical layer (C-PHY) switching jitter.

21. The method of claim 20, wherein the causing comprises reducing the channel physical layer (C-PHY) switching jitter by adjusting a switching timing for the plurality of data signals based on the delay.

22. The method of claim 14, wherein the transmitting comprises transmitting the plurality of data signals compliant with MIPI® channel physical layer (C-PHY).

CLAIMS

We claim:

1. An apparatus, comprising:

a pattern dependent delay circuit including:

a pattern detector to detect a switching pattern of at least three data signals on respective wires; and

a delay module coupled to the pattern detector to adaptively change delays of the at least three data signals based on the detected switching pattern; and

a transmitter, coupled to the pattern dependent delay circuit, to transmit the at least three data signals.

2. The apparatus of claim 1, wherein individual data signals of the at least three data signals switch between at least three logic states.

3. The apparatus of claim 2, wherein the at least three data signals are in different logic states.

4. The apparatus of claim 2, wherein the pattern detector is to detect the switching pattern based on a prior logic state and a current logic state of the at least three data signals.

5. The apparatus of claim 1, wherein the pattern detector is to send one or more control signals to the delay module to change the delays of the at least three data signals when the pattern detector detects that the at least three data signals are each undergoing a state transition during a same time period.

6. The apparatus of claim 1, wherein the delay module is to cause different delays for each of the at least three data signals.

7. The apparatus of claim 1, wherein the delay module comprises a plurality of delay controllers and a plurality of samplers, wherein individual delay controllers are paired with individual samplers to cause delay of respective individual data signals of the at least three data signals.

8. The apparatus of claim 1, wherein the pattern dependent delay circuit is to adaptively change the delays of the at least three data signals before the transmitter transmits the at least three data signals to reduce a switching jitter associated with the at least three data signals.

9. The apparatus of claim 1, wherein the pattern dependent delay circuit is to reduce a channel physical layer (C-PHY) switching jitter.

10. The apparatus of claim 1, wherein the transmitter is a mobile industry processor interface (MIPI) channel physical layer (C-PHY) compliant transmitter.

11. A system, comprising:

a processor;

a controller coupled to the processor to output data processed by the processor;

a transmitter coupled to the controller to transmit the data using at least three data signals, wherein individual data signals of the at least three data signals switch between at least three logic states; and

a pattern dependent delay circuit, coupled to the transmitter, to detect a switching pattern of the at least three data signals and adaptively reduce a switching jitter based on the detected switching pattern.

12. The system of claim 11, wherein the pattern dependent delay circuit is to reduce a channel physical layer (C-PHY) switching jitter by changing delays on the at least three data signals before the transmitter transmits the at least three data signals.

13. The system of claim 11, wherein the transmitter is a MIPI® channel physical layer (C-PHY) compliant transmitter.

14. A method, comprising:

detecting a switching pattern of a plurality of data signals on respective wires;

causing a delay on one or more of the plurality of data signals based on the detected switching pattern; and

transmitting the plurality of data signals.

15. The method of claim 14, wherein the detecting comprises detecting a logic state of individual data signals of the plurality of data signals, wherein the logic state is one of at least three possible logic states.

16. The method of claim 14, wherein the detecting comprises detecting the switching pattern based on a prior logic state and a current logic state of the plurality of data signals.

17. The method of claim 14, wherein the causing the delay is responsive to a detection that each of the plurality of data signals switches to a different logic state from a prior logic state.

18. The method of claim 14, wherein the causing comprises changing delays on each of the plurality of data signals based on the switching pattern.

19. The method of claim 14, wherein the causing comprises causing different delays on each of the plurality of data signals based on the switching pattern.

20. The method of claim 14, wherein the causing comprises reducing a channel physical layer (C-PHY) switching jitter.

21. The method of claim 20, wherein the causing comprises reducing the channel physical layer (C-PHY) switching jitter by adjusting a switching timing for the plurality of data signals based on the delay.

22. The method of claim 14, wherein the transmitting comprises transmitting the plurality of data signals compliant with MIPI® channel physical layer (C-PHY).