

ABSTRACT

[0096] A three-dimensional semiconductor memory device, including a first chip and a second chip stacked on the first chip may be provided. The first chip may include a first substrate including a first peripheral circuit region and a second peripheral circuit region, first contact plugs, and second contact plugs, and a passive device on and electrically connected to the second contact plugs. The second chip may include a second substrate including a cell array region and a contact region, which vertically overlap the second peripheral circuit region and the first peripheral circuit region of the first chip, respectively. The second chip may further include gate electrodes, and cell contact plugs disposed on the contact region of the second substrate and on end portions of the gate electrodes. The first passive device may be vertically between the gate electrodes and the second contact plugs and may include a first contact line.

FIG. 4