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(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 South Federal Way, Boise, ID 83716-9632 (US).

(72) Inventor: **FORBES, Leonard**; 965 NW Highland Ter-
race, Corvallis, OR 97330 (US).

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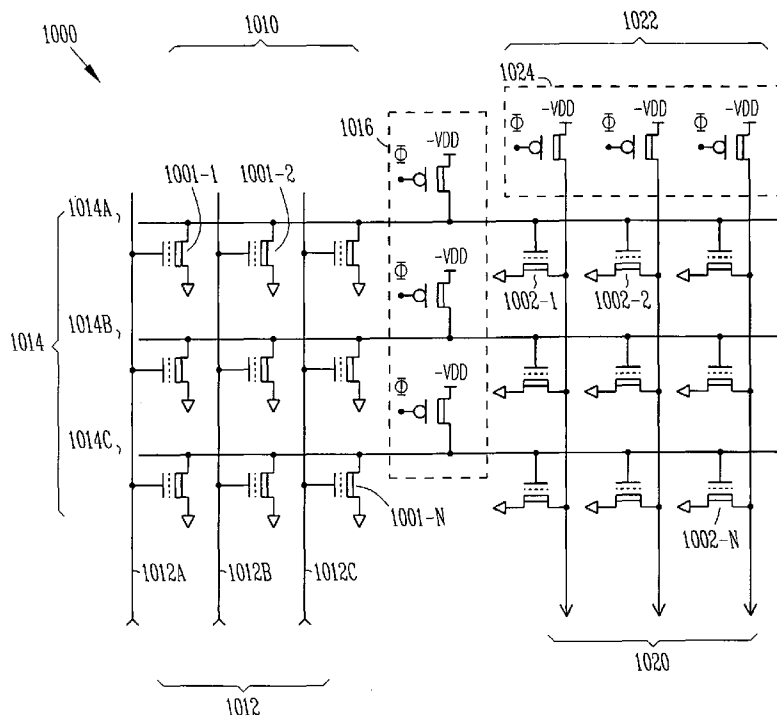
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(74) Agent: **VIKSINS, Ann, S.**; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

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(54) Title: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH ULTRA THIN VERTICAL BODY TRANSISTORS



(57) Abstract: Structures and methods for in service programmable logic arrays with ultra thin vertical body transistors are provided. The in-service programmable logic array includes a first logic plane that receives a number of input signals. The first logic plane has a plurality of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs. A second logic plane has a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the in service programmable logic array implements a logical function. Each of the logic cells includes a vertical pillar extending outwardly from a semiconductor substrate. Each pillar includes a single crystalline first contact layer and a second contact layer separated by an oxide layer. At least one single crystalline ultra thin vertical floating gate transistor that is disposed adjacent each vertical pillar. The single crystalline vertical floating

gate transistor includes an ultra thin single crystalline vertical first source/drain region coupled to the first contact layer, an ultra thin single crystalline vertical second source/drain region coupled to the second contact layer, and an ultra thin single crystalline vertical body region which opposes the oxide layer and couples the first and the second source/drain regions. A vertical floating gate opposes the ultra thin single crystalline vertical body region.

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