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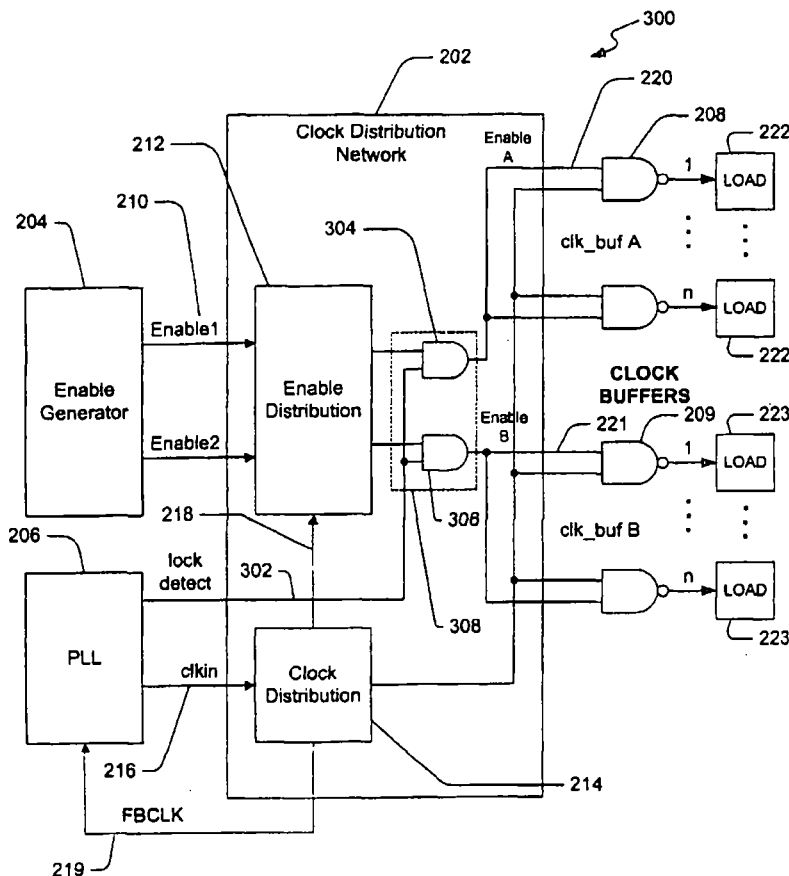
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(54) Title: APPARATUS FOR SELECTIVELY DISABLING CLOCK DISTRIBUTION



(57) Abstract: A clock distribution network includes a phase-locked loop (PLL), clock buffers, an enabling circuit, and a distribution inhibit circuit. The PLL is configured to generate a clock signal and a lock detect signal. The clock buffers are adapted to receive the clock signal from the PLL. The buffers have outputs that can be connected to clock loads. The enabling circuit enables selected buffers to drive the clock loads. The distribution inhibit circuit selectively produces the enable signal to inhibit distribution of the clock signal responsive to the lock detect signal.

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