

METHODS TO IMPROVE THERMAL STABILITY AND FILM CRACKING MARGIN FOR LOW TEMPERATURE HIGH TENSILE SILICON NITRIDE THIN FILMS

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

BACKGROUND

[0002] In semiconductor processing, it may be desired that a wafer remains substantially flat. However, during normal operations, a wafer may experience wafer bow. The wafer bow may cause issues such as improper clamping by an electrostatic chuck, inability to be held by a wafer handler, pattern transfer issues during photolithography issues, and others. Processes have been developed to manage wafer bow by keeping the wafer flat within process tolerances. One process includes depositing a film on the backside of the wafer to counteract any stress that may be causing the wafer to bow.

[0003] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor implicitly admitted as prior art against the present disclosure.

SUMMARY

[0004] Disclosed herein are methods and systems of depositing films. In one aspect of the embodiments herein, a method of reducing bow in a substrate is provided, the method including: receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the one or more frontside layers induce a bow in the substrate; depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing; depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type.

[0005] In some embodiments, the first backside layer includes more silicon-hydrogen bonds than the second backside layer. In some embodiments, the method further includes annealing

the substrate, wherein a combined internal stress of the first backside layer and the second backside layer changes by less than 10% after annealing. In some embodiments, annealing occurs at a temperature greater than about 700 °C. In some embodiments, depositing the first backside layer and depositing the second backside layer are performed at temperatures less than about 500°C. In some embodiments, a rate of depositing the first backside layer or the second backside layer is at least about 300Å per minute. In some embodiments, the first type of internal stress shift is a tensile stress shift. In some embodiments, the second type of internal stress shift is a compressive stress shift. In some embodiments, the first backside layer and second backside layer include silicon nitride. In some embodiments, the first backside layer and second backside layer each have an intrinsic internal stress magnitude of about 100 MPa to 1000 MPa. In some embodiments, the first backside layer and second backside layer both have a tensile internal stress. In some embodiments, the bow of the substrate is about 300µm or more. In some embodiments, the bow of the substrate after depositing the first backside layer and the second backside layer is less than about 100 µm. In some embodiments, at least one of the one or more frontside layers includes a hardmask. In some embodiments, the one or more frontside layers include a stack of about 100 or more alternating layers. In some embodiments, the stack includes alternating oxide layers and nitride or polysilicon layers. In some embodiments, the first backside layer and second backside layer have a thickness of about 0.1 µm to about 5 µm.

[0006] In another aspect of the embodiments herein, a substrate is provided, the substrate including: one or more frontside layers on a frontside of the substrate; a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing; a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type. In some embodiments, if from the one or more frontside layers are not compensated by the first backside layer, the substrate has a bow of about 300 µm or more. In some embodiments, the first type of internal stress shift is tensile and the second type of stress shift is compressive. In some embodiments, if from the one or more frontside layers are not compensated by the first backside layer, the substrate has a bow of about 300 µm or more. In some embodiments, the first backside layer and second backside layer include silicon nitride. In some embodiments, the first backside layer and second backside layer have a thickness of about 0.1 µm to about 5 µm. In some embodiments, the first backside layer includes more silicon-hydrogen bonds than the second backside layer. The substrate of claim 18, wherein a combined internal stress of the first backside layer and the second backside layer, if annealed, changes by less than 10% after annealing.

[0007] In another aspect of the embodiments herein, an apparatus for semiconductor processing is provided, the apparatus including: a process chamber; and a controller including memory and processors configured for: receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the one or more frontside layers induce a bow in the substrate; depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing; depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type.

[0008] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Figures 1A and 1B show examples of unbowed and bowed semiconductor wafers on an electrostatic chuck.

[0010] Figures 2A-C show examples of stress shifts following thermal treatments.

[0011] Figure 3 is an FTIR spectra of two different films having a tensile stress shift and a compressive stress shift following annealing.

[0012] Figure 4 is a table of film internal stress properties corresponding to the films shown in Figure 3.

[0013] Figure 5 is a process flow diagram illustrating certain operation in semiconductor wafer processing.

[0014] Figures 6A and 6B show a block diagram of an example substrate processing system.

[0015] Figure 7A shows an example cross section of an edge of a shower-pedestal.

[0016] Figure 7B shows a top view of an example carrier ring.

[0017] Figure 8 shows a schematic of an example process system that may be used to perform the methods described herein.

DETAILED DESCRIPTION

Terminology

[0018] The following terms are used throughout the instant specification:

[0019] The terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate” and “partially fabricated integrated circuit” may be used interchangeably. Those of ordinary skill in the art understand that the term “partially fabricated integrated circuit” can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A

wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the like. The workpiece may be of various shapes, sizes, and materials.

[0020] A “semiconductor device fabrication operation” as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and material additive processes, such as deposition processes (e.g., physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0021] “Manufacturing equipment” refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0022] “Wafer bow” as used herein may refer to a deformation of a wafer. The deformation may have radial and/or azimuthal components. Examples of types of wafer bow include dome shapes, bowl shapes, and saddle shapes. Wafer bow may occur during fabrication, for example, as a result of stress to the wafer during deposition of materials on an active surface of a wafer substrate. Wafer bow may occur during various types of fabrication, such as when large stacks of materials are deposited. Wafer bow may cause complications in subsequent processing

steps. For example, the wafer may fail to chuck correctly if an amount of bowing is too large. Moreover, some processing steps (e.g., photolithography) may produce poor results if performed on a wafer that is excessively bowed.

[0023] Wafer bow may be measured as a deviation of the mean or median distance of the surface of the wafer to a reference plane. In some embodiments, the point of the median surface of the wafer may be the center point (e.g., in the case of concave or domed bowing), or an edge point of the wafer and/or an average edge point of the wafer (e.g., in the case of warping or convex bowing). In some embodiments wafer bow may be measured from a reference plane such that when an edge point of the wafer is below the reference plane the edge point is considered to have a negative bow, and when the edge point of the wafer is above the reference plane the edge point is considered to have a positive bow. In some embodiments, positive or negative bow may be measured along a z axis perpendicular to the reference plane.

Bowed Wafers

[0024] Semiconductor device fabrication often involves deposition of a stack of layers on a wafer substrate. Typically, most deposition and other processing to form the devices occurs on one side of the substrate, often referred to as the front face or frontside of a wafer. As the deposited layers build up, they can introduce stress in the wafer. A large net tensile or compressive stress can cause the wafer to bow, which is undesirable.

[0025] Bowing is especially likely to occur where large stacks of materials are deposited, for example, in the context of 3D-NAND devices, or where a thick front side layer is deposited. Where bowing is significant, it can deleteriously affect subsequent processing steps. For instance, the wafer may fail to chuck correctly if the bowing is too great. Figures 1A and 1B show a wafer on an electrostatic chuck. Figure 1A shows a wafer 102 on an electrostatic chuck 110. When the wafer 102 is substantially flat for purposes of a particular process operation, e.g., having a bow of about 100 μm or less, the wafer may be properly clamped, securing the wafer for subsequent processing steps. Figure 1B shows a bowed wafer 104 on the electrostatic chuck 110. When the bow is significant, the wafer may fail to secure properly on the electrostatic chuck. Wafer bow may cause other problems. For example, certain processing steps (e.g., photolithography) are very precise and produce poor results if the wafer is not substantially flat. The problem may be manifest as lithography defocus.

[0026] One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride, etc.). Another example of a type of stack likely to cause bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples

of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride.

[0027] The materials in the stacks may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material present on the frontside of the wafer.

[0028] The frontside stacks may be deposited to any number of layers and thicknesses. In an example, the stack includes about 20 or more layers, and has a total thickness of about 2 μm to about 4 μm . However, in some cases, multiple-layer stacks have about one hundred or more layers. In some embodiments, multiple-layer stacks may have about five hundred or more layers. In some embodiments, the multiple-layer stacks may have about one thousand or more layers. Such stacks may have a thickness of about 4 μm to 12 μm , for example.

[0029] The stress induced in the wafer by the stack or other frontside deposition may be about -500 MPa to about $+500$ MPa. In some embodiments, the resulting in a bow is about 150 μm or greater, e.g., about 300 μm and above, about 400 μm and above, or about 200 μm to about 400 μm (for a 300 mm wafer).

[0030] Another cause of wafer bow may be frontside processing which uses thick hardmasks with limited etch selectivity. In these embodiments, at least one of the one or more frontside layers is a hardmask. The thick hardmasks may have an internal stress similar to those described above, e.g., have a magnitude of 0 MPa to about 500 MPa. The stress caused by the hardmask may be tensile stress or compressive. The thick hardmasks may cause wafers to have a significant wafer bow, e.g., about 150 μm or more.

[0031] Various techniques have been devised for combatting bowing. When bowing is more severe, deposition processes may be tuned to reduce or counteract internal stresses in deposited layers. However, any such tuning should not interfere with process requirements for fabricating devices. One commonly used technique to counteract bowing deposits a film on the back side of the wafer.

[0032] Backside deposition may form a high-stress film. If the backside layer has the same type of internal stress (tensile or compressive) and of comparable magnitude to the internal stress created on the frontside, the backside film effectively counteracts and reduces the bow.

[0033] Examples of backside films used to counteract bow include the following: amorphous

silicon, silicon oxide, silicon nitride, and silicon oxynitride. Current backside films have high internal stress and can mitigate the stresses imparted on the wafer from the frontside layers to reduce or eliminate the wafer bow. Generally, backside layers are made of films with high stress.

[0034] Until relatively recently, the backside film thickness remained relatively thin (e.g., <1 μ m) because the bow caused by depositing material on the frontside was relatively modest. Thus, downstream processes at previous technology nodes did not normally experience issues addressed by embodiments herein. However, modern IC fabrication techniques may produce substrates having frontside layers that produce much more severe wafer bow compared to previous nodes. For example, some modern processes use thick hardmask layers in operations where the etch selectivity between the hardmask and etched material is limited, yet deep trenches or vias are etched. In another example, frontside stacks have increased the number of layers. For example, in previous nodes stacks may have been about 32 to about 72 layers. Now, stacks may have hundreds or even thousands of layers, increasing the thickness of the frontside layer and the internal stress. Typically wafer bow compensation is achieved by depositing a single backside layer. Due to the increasing magnitude of wafer bow, thicker backside films must be deposited to compensate for wafer bow. This has caused certain issues. Due to large internal forces occurring within thick backside layers, the layers may spontaneously form film cracks. For many film materials (e.g., tensile silicon nitride films), cracks are observed in films of thicknesses necessary to compensate for bow values above a critical bow limit. These bow limits are commonly known as the “bow cracking limit” or “cracking margin.”

[0035] In some implementations, backside films may be deposited at a high temperature having a large internal tensile stress to compensate for tensile internal stress of the frontside layers. However, in some embodiments the backside layers may need to be deposited at lower temperatures to avoid annealing one or more frontside layers, e.g., a hardmask layer used for etching. In some implementations, the backside films to counteract wafer bow are deposited at low temperatures, e.g., temperatures below 400°C. During subsequent processing the hardmask layer may be removed and a higher temperature process may be performed, which may anneal the backside films. The backside films may experience a shift in internal stress during an annealing operation or thermal treatment at a high temperature, e.g., above 800°C. This stress shift may either increase the internal tensile stress above the cracking margin, causing failure of the backside film, or decrease the internal tensile stress, reducing the amount of wafer bow that the backside film may compensate. The internal stress shift is generally undesirable as an

additional deposition process may be required to properly compensate for wafer bow after the internal stress of the prior backside films shifts during an operation that anneals the backside films. This adds complexity to device manufacturing and decreases overall throughput.

BACKSIDE FILM INTERNAL STRESS SHIFT COMPENSATION

[0036] Disclosed herein are methods, systems, and techniques for maintaining the internal stress of backside layers deposited at low temperature deposition conditions and subsequently annealed at high temperatures. This reduces the need for additional backside film deposition, reduces the risk of a wafer handling problem during subsequent wafer processing, and maintains wafer bow compensation after annealing without cracking of the backside films.

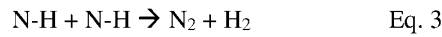
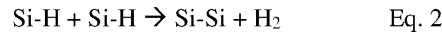
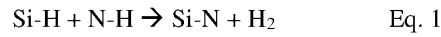
[0037] Figure 2A and 2B illustrate layers having a tensile stress shift and a compressive stress shift, respectively. In Figure 2A, a substrate 200 has a tensile stress shift layer 211a having an internal tensile stress (hence the “bowl” shape). A wafer bow 203 is shown as a deflection from the center to edge of the substrate, and may be measured along an axis normal to a plane tangent to the minima of the curve of the wafer (i.e., solid line shown). Following a thermal cycle, annealed tensile stress shift layer 211a has cracked, as shown by cracked layer 211b having cracks 213. As a result, substrate 200a may have a lower wafer bow 204a as the cracked layer 211b has reduced its internal stress by a cracking failure. In some embodiments, cracking may not necessarily affect wafer bow, e.g., wafer bow 204a may be much closer to or the same as wafer bow 203, but cracking may cause defects and compromise the film integrity. For example, during a downstream wet chemistry process, species may diffuse into the cracks and cause undesirable reactions.

[0038] In Figure 2B, substrate 200 has a compressive stress shift layer 215a having an internal tensile stress and wafer bow 203, similar to Figure 2A. After a thermal cycle, annealed compressive stress shift layer 215b has a lower internal tensile stress and thus a reduced wafer bow 204 for substrate 200b. In both Figure 2A and 2B, the internal stress shift following annealing has reduced the ability of the backside films to counteract wafer bow. It should be understood that for both Figures 2A and 2B (and also 2C) that greater wafer bow is indicative of a greater ability of the backside film to counteract wafer bow from frontside layers. Backside films may be deposited on flat wafers and the resulting wafer bow indicates how much wafer bow the backside films may counteract when deposited on substrates having frontside layers that cause bowing and are thus already bowed.

[0039] To address this concern, in some embodiments a combination of compressive stress shift and tensile stress shift layers may be deposited. By depositing both types of layers, the wafer bow may be properly compensated for prior and subsequent to an annealing operation,

as the internal stress shifts of each type of layer counteract each other. Figure 2C illustrates this with substrate 200 having a tensile stress shift layer 217a and a compressive stress shift layer 219a, and a wafer bow 203. After a thermal cycle substrate 200c has substantially the same wafer bow 204c. Tensile stress shift layer 217b has not cracked, and the greater internal tensile stress of annealed tensile stress shift layer 217b has been counteracted by the reduced internal tensile stress of annealed compressive stress shift layer 219b. In some implementations, compressive stress shift layer 219a may be deposited on tensile stress shift layer 217a so that annealed compressive stress shift layer 219b may counteract and inhibit cracking of annealed tensile stress shift layer 217b. In some embodiments, if tensile stress shift layer 217a is the last deposited backside film it may still crack at the surface due to increased local internal stress.

[0040] The mechanism of internal stress shift under annealing conditions may relate to the proportions of N-H, Si-H, and Si-N bonds in the films. Figure 3 illustrates FTIR spectra of two example films according to various embodiments herein, film A and film B. Film A is a tensile stress shift film and film B is a compressive stress shift film; Figure 4 presents a table of internal stress pre- and post-anneal for each film. As shown in Figure 3, Film A has a lesser proportion of N-H bonds 302 and a greater proportion of Si-H 304 and Si-N bonds 306 than Film B. During annealing, three different reactions may take place:



[0041] The kinetics of each reaction may depend on the proportion of each type of bond in the films. Thus, if there is a significant proportion of Si-H and N-H bonds, Eq. 1 may have a greater reaction rate and thus an increased formation of Si-N, which may increase the internal tensile stress of the film. Conversely, if the proportion of Si-H or N-H is low, then the reaction rate of equation 1 will be lower and equations 2 and 3 may have a proportionally larger reaction rate, which results in a compressive internal stress shift.

[0042] H_2 and N_2 that are formed from the reactions above during annealing may leave the film as gasses, thus these reactions may be substantially irreversible. During initial film deposition hydrogen may become trapped in the film as part of the bonds shown, and during an anneal or high temperature treatment the higher temperature may drive these reactions to remove additional hydrogen from the film, causing the internal stress shifts depending on the relative proportions of each type of bond and thus the reaction rate for each equation. After sufficient time under anneal conditions the proportion of hydrogen in the film may be sufficiently reduced to reduce the reaction rates substantially, such that additional annealing

does not further change the internal stress.

[0043] The presence of hydrogen in the film may result from a low deposition temperature. Typically, a SiN film as disclosed herein may be deposited at a high temperature, e.g., greater than about 700°C or about 800°C, to drive the reactions above and remove hydrogen from the film. However, in some implementations backside films may be deposited to compensate for wafer bow under process condition constraints that limit the maximum temperature for the backside film deposition process, e.g., less than about 450°C, less than about 500°C, less than about 550°C, or less than about 600°C. For example, frontside layers may undesirably anneal under high temperature conditions, and thus the backside film deposition conditions may be limited in the maximum temperature. The lower temperature backside layer deposition may introduce hydrogen into the film that will then react during subsequent operations where the maximum temperature constraint is no longer present and a higher temperature process is desirable.

[0044] The proportion of Si-N, Si-H, and N-H bonds may be controlled by deposition conditions of the silicon nitride films, particularly the relative flow rates of silicon-containing precursors and nitrogen-containing precursors. While hydrogen is difficult to remove from the film without an anneal treatment, the proportions of each type of bond may be controlled. Increasing the relative proportion of silicon-containing precursors to nitrogen-containing reactants may increase the proportion of Si-H bonds in the resulting film, increasing the reaction rate of equation 1 during a subsequent anneal, resulting in a tensile stress shift film. Conversely, decreasing the relative proportion of silicon-containing precursors to nitrogen-containing reactants would decrease the proportion of Si-H bonds in the resulting films and decrease the reaction rate of equation 1 in favor of equations 2 and/or 3, resulting in a compressive stress shift film. In some embodiments, the proportion of silicon-containing precursors to a nitrogen-containing reactant, e.g., NH₃, may vary between 2:1 and 1:100, where a 2:1 ratio would result in a tensile stress shift film, and a ratio of 1:100 would result in a compressive stress shift film. It should be understood that other gases may also be flowed, including inert gases such as N₂ or Ar that help stabilize a plasma that is ignited as part of a deposition process for films disclosed herein but otherwise do not react with the depositing film.

[0045] Figure 4 presents a table of film properties for example films A, B, and A+B as shown in the FTIR spectra of Figure 3. Film A is a tensile stress shift film, as shown by the increased film stress after an anneal operation. The last column indicates the maximum wafer bow that the film may compensate without cracking after annealing. Because of the increasing tensile internal stress shift of film A after annealing, film A can only compensate for 170 µm of wafer

bow as otherwise it would crack following the tensile stress shift. Film B, conversely, has a compressive internal stress shift (negative stress is compressive), which similarly limits the wafer bow it may compensate as after annealing it loses its internal stress. Depositing the compressive internal stress shift film to have a higher initial bow would cause it to crack before annealing, similar to the tensile internal stress shift film cracking after annealing.

[0046] By combining films A and B, the stress shifts of both films may be tuned to offset each other. As shown by film A+B, the combined film stress pre- and post-anneal is substantially the same, allowing for the backside films to compensate for wafer bow under both conditions. As the bilayer film's stress does not substantially change after annealing, the maximum wafer bow it may compensate for is much higher as it does not crack like film A or have a reduced tensile stress like film B. It should be understood that the thickness of both films does not need to be the same; in the table of Figure 4 Film A may make up less than the total thickness of film A+B than film B, as film A has a greater magnitude in internal stress shift after annealing than film B. Tuning the ratio of thicknesses of both films and the stress shifts of both films may result in a stress shift of the bilayer of less than about 10%, less than about 5%, less than about 2%, or less than about 1%. The films shown in Figure 4 have a thickness of 3000A for film A, 11000A for film B, and 9000A for film A+B. In some embodiments, the thickness of a film and the bow it may compensate are directly correlated; the internal stress may be constant and film thickness is varied to compensate more or less wafer bow. In various embodiments herein, the thicknesses of backside films disclosed herein may be between about 0.1 and about 5 μm .

[0047] Figure 5 shows an example process of deposition of a backside layer structure including two or more films have different stress shifts. The process of Figure 5 starts with depositing one or more frontside layers having a first type of internal stress, e.g., a tensile internal stress (502). The wafer may have one or more frontside layers deposited thereon that cause bowing of the wafer.

[0048] Once the frontside layer(s) are deposited onto the wafer, one or more first backside layers having the first type of internal stress are deposited onto the wafer (504). The internal stress of the first backside layer counteracts the internal stress from the frontside layer and may help reduce wafer bow. This first backside layer may have a tensile stress shift, i.e., under annealing conditions the internal stress of the layer may increase (become more tensile).

[0049] One or more second backside layers are deposited on the first backside layer having the first type of internal stress (506). The second backside layer has an internal stress that is the same as the internal stress of the frontside layer and the first backside layer, but has an

opposite stress shift under annealing conditions, e.g., the internal stress of the layer may decrease (become more compressive).

[0050] Both the first and second backside layers may be deposited at a low temperature, e.g., less than about 400°C, less than about 450°C, less than about 500°C, less than about 550°C, or less than about 600°C. At such deposition temperatures a significant amount of hydrogen is incorporated into the layers, which may then react and cause a tensile or compressive stress shift during subsequent high temperature conditions, e.g., greater than about 700°C, greater than about 800°C, or greater than about 900°C.

[0051] In some embodiments, the deposition rate for the backside layers disclosed herein may range between about 300Å to about 800Å per minute. Low temperature deposition films may typically have additional hydrogen content to maintain such deposition rates. While the hydrogen content of backside films may be reduced, and thus the magnitude of any internal stress shifts may similarly be reduced, the deposition rate of such films may be a fraction of those noted above. This may be due to requiring an extremely low partial pressure of silane precursors to reduce the hydrogen content when depositing at low temperatures. Thus, techniques disclosed herein may allow for a greater deposition rate while maintaining a neutral stress shift under subsequent anneal conditions.

[0052] After deposition of the first and second backside layers, the substrate may undergo a fabrication operation at a temperature that causes the first and second backside layers to have a stress shift. While the first backside layer and the second backside layer may individually experience an internal stress shift, the combined internal stress from both films remains substantially the same, e.g., the internal stress of the combined first and second backside layers changes by less than about 10%, less than about 5%, less than about 2%, or less than about 1%.

[0053] In some embodiments, the magnitude of the internal stress of the deposited first and second backside layers may be less than the magnitude of the internal stress of the deposited frontside layer; i.e., the first and second backside layers do not fully compensate the bow induced by the frontside layer(s). In some embodiments, the first and second backside layer reduces the bow of the wafer to about 200 μm or less.

[0054] The backside layers may be deposited using CVD, PECVD, ALD, epitaxy, PVD, or other deposition processes. The backside layers may be deposited using a special purpose backside deposition apparatus. The backside deposition apparatus may be a different deposition apparatus than the apparatus used to deposit the one or more frontside layers.

[0055] The bow induced by the first and second backside layers may be the sum of the individual induced bows. In some embodiments, bow magnitude of the combined backside

layers may be about the same as the bow magnitude of the one or more frontside layers. In some embodiments, the bow contributions of all frontside and backside layers may combine so that the total bow of the wafer is minimal (i.e., less than about 100 μm .) In some embodiments, after performing the method of Figure 5, the wafer may be substantially flat, e.g., the wafer has a bow of about 200 μm or less, about 150 μm or less, or about 100 μm or less.

[0056] Note that references to bow values induced or caused by individual backside layers assume that the bow is uncompensated by other layers. For example, when referring to the magnitude of a bow caused by a first backside layer, we assume that is the bow that would be produced on the substrate if no other layers were present, e.g., no frontside layers. The magnitude of a bow induced by a layer depends on both the internal stress of the material in the layer and the thickness of the layer.

[0057] Compensation by backside layers refers to bow contributions of backside layers that may combine with bow contributions of frontside layers to reduce or equalize wafer bow. As noted above, bow contributions of all frontside and backside layers may be combined. A positive bow caused by frontside layers, forming a bowl shape, may be caused by frontside layers having a tensile internal stress. This bow may be reduced by a backside layer also having a tensile internal stress that causes an opposite, negative bow. The negative bow caused by the backside layer compensates the positive bow caused by the frontside layers, resulting in a total bow of the wafer that is minimal. In some embodiments, compensation may include partially mitigating wafer bow. As noted above, a first backside layer and second backside layer may partially compensate wafer bow. In other embodiments, a first backside layer and a second backside layer may fully compensate wafer bow, e.g., reduce wafer bow to less than about 100 μm .

[0058] In certain embodiments, backside layer disclosed herein comprise a material having an intrinsic internal stress, which has a magnitude of at least about 100 MPa or about 100 to about 2000 MPa. These values may be for tensile or compressive internal stress, as the case may be for the type of backside material needed to counteract bow caused by the frontside layer(s). The above-recited internal stress values may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may have the same or different values of internal stress.

[0059] Example materials used to make backside layers having tensile internal stress include silicon nitrides (SiN), silicon oxynitrides, and polymer layers. As examples, tensile films can be deposited using CVD or PECVD techniques. To combat wafer bow caused by a frontside layer with a compressive internal force, a compressive film may be used for the bulk backside

layers. Compressive films may be formed using specific materials and/or processing conditions. Example materials used to make compressive films include silicon oxides (SiO_x), silicon nitrides, aluminum oxides, aluminum nitrides, and polysilicon. Compressive films can be deposited using CVD or PECVD techniques. The above-recited materials and deposition techniques may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may be formed by the same or different techniques.

[0060] Backside films disclosed herein may be deposited using PECVD techniques using silicon-containing precursors and nitrogen-containing reactants. The internal stress shift of films may be tuned to either tensile or compressive, and the magnitude of such shifts may also be tuned by control of various process parameters. Such process parameters may include temperature, pressure, species flow rates, plasma power, etc. Tuning a single backside film to have either a compressive or tensile stress shift is generally easier than tuning the backside films to have a neutral stress shift, as the hydrogen content and what the hydrogen is bonded to may substantially affect the type and magnitude of stress shift. Furthermore, the relative thicknesses of each backside layer may be tuned so that the stress shift for each film is substantially equal in magnitude and opposite in sign. In some implementations, the ratio of silicon-precursors to nitrogen-containing reactants may be between about 2:1 and about 1:100, where a greater proportion of silicon precursors may cause the film to have a more tensile stress shift. Other gaseous species may also be co-flowed, including inert gases.

[0061] For depositing silicon-containing films, one or more silicon-containing precursors may be used. In some examples, silicon-containing precursors can include silanes (e.g., SiH_4), polysilanes ($\text{H}_3\text{Si}-(\text{SiH}_2)_n-\text{SiH}_3$) where $n \geq 1$, organosilanes, halogenated silanes, aminosilanes, alkoxysilanes, and the like. Organosilanes such as methylsilane, ethylsilane, isopropylsilane, t-butylsilane, dimethylsilane, diethylsilane, di-t-butylsilane, allylsilane, *sec*-butylsilane, hexylsilane, isoamylsilane, t-butylidisilane, di-t-butylidisilane, and the like.

[0062] A halosilane includes at least one halogen group and may or may not include hydrogens and/or carbon groups. Examples of halosilanes are iodosilanes, bromosilanes, chlorosilanes, and fluorosilanes. Specific chlorosilanes are tetrachlorosilane, trichlorosilane, dichlorosilane, monochlorosilane, chloroallylsilane, chloromethylsilane, dichloromethylsilane, chlorodimethylsilane, chloroethylsilane, t-butylchlorosilane, di-t-butylchlorosilane, chloroisopropylsilane, chloro-*sec*-butylsilane, t-butyl dimethylchlorosilane, hexyldimethylchlorosilane, and the like.

[0063] An aminosilane includes at least one nitrogen atom bonded to a silicon atom, but may also contain hydrogens, oxygens, halogens, and carbons. Examples of aminosilanes are mono-

, di-, tri- and tetra-aminosilane ($\text{H}_3\text{Si}(\text{NH}_2)$, $\text{H}_2\text{Si}(\text{NH}_2)_2$, $\text{HSi}(\text{NH}_2)_3$ and $\text{Si}(\text{NH}_2)_4$, respectively), as well as substituted mono-, di-, tri- and tetra-aminosilanes, for example, t-butylaminosilane, methylaminosilane, tert-butylsilanamine, bis(tert-butylamino)silane ($\text{SiH}_2(\text{NHC}(\text{CH}_3)_3)_2$ (BTBAS), tert-butyl silylcarbamate, $\text{SiH}(\text{CH}_3)-(\text{N}(\text{CH}_3)_2)_2$, $\text{SiHCl}-(\text{N}(\text{CH}_3)_2)_2$, $(\text{Si}(\text{CH}_3)_2\text{NH})_3$, di-isopropylaminosilane (DIPAS), di-sec-butylaminosilane (DSBAS), $\text{SiH}_2[\text{N}(\text{CH}_2\text{CH}_3)_2]_2$ (BDEAS) and the like. A further example of an aminosilane is trisilylamine ($\text{N}(\text{SiH}_3)$). In some embodiments, an aminosilane that has two or more amine groups attached to the central Si atom may be used. These may result in less damage than aminosilanes having only a single amine group attached.

[0064] Further examples of silicon-containing precursors include trimethylsilane (3MS); ethylsilane; butasilanes; pentasilanes; octasilanes; heptasilane; hexasilane; cyclobutasilane; cycloheptasilane; cyclohexasilane; cyclooctasilane; cyclopentasilane; 1,4-dioxo-2,3,5,6-tetrasilacyclohexane; diethoxymethylsilane (DEMS); diethoxysilane (DES); dimethoxymethylsilane; dimethoxysilane (DMOS); methyl-diethoxysilane (MDES); methyl-dimethoxysilane (MDMS); octamethoxydodecasiloxane (OMODDS); tert-butoxydisilane; tetramethylcyclotetrasiloxane (TMCTS); tetraoxymethylcyclotetrasiloxane (TOMCTS); triethoxysilane (TES); triethoxysiloxane (TRIES); and trimethoxysilane (TMS or TriMOS).

[0065] In some implementations silicon-containing precursors may include siloxanes or amino-group-containing siloxanes. In some embodiments, siloxanes used herein may have a formula of $\text{X}(\text{R}^1)_a\text{Si}-\text{O}-\text{Si}(\text{R}^2)_b\text{Y}$, where a and b are integers from 0 to 2, and X and Y independently can be H or NR^3R^4 , where each of R1, R2, R3 and R4 is hydrogen, unbranched alkyl, branched alkyl, saturated heterocyclic, unsaturated heterocyclic groups, or combinations thereof. In some embodiments, when at least one X or Y is NR^3R^4 , R3 and R4, taken together with the atom to which each are attached, form a saturated heterocyclic compound. In some embodiments, the silicon-containing precursors are pentamethylated amino group containing siloxanes or dimethylated amino group containing siloxanes. Examples of amino group containing siloxanes include: 1-diethylamino 1,1,3,3,3-pentamethyl disiloxane, 1-diisopropylamino-1,1,3,3,3-pentamethyl disiloxane, 1 dipropylamino-1,1,3,3,3-pentamethyl disiloxane, 1-di-n-butylamino-1,1,3,3,3-pentamethyl disiloxane, 1-di-sec-butylamino-1,1,3,3,3-pentamethyl disiloxane, 1-N-methylethylamino 1,1,3,3,3-pentamethyl disiloxane, 1-N-methylpropylamino-1,1,3,3,3-pentamethyl disiloxane, 1 N-methylbutylamino -1,1,3,3,3-pentamethyl disiloxane, 1-t-butylamino -1,1,3,3,3-pentamethyl disiloxane, 1-piperidino-1,1,3,3,3-pentamethyl disiloxane, 1-dimethylamino-1,1-dimethyl disiloxane, 1-diethylamino-

1,1-dimethyl disiloxane, 1-diisopropylamino-1,1-dimethyl disiloxane, 1-dipropylamino-1,1-dimethyl disiloxane, 1-di-n-butylamino-1,1-dimethyl disiloxane, 1-di-sec butylamino-1,1-dimethyl disiloxane, 1-N-methylethylamino-1,1-dimethyl disiloxane, 1-N-methylpropylamino-1,1-dimethyl disiloxane, 1-N-methylbutylamino-1,1-dimethyl disiloxane, 1-piperidino-1,1-dimethyl disiloxane, 1-t-butylamino-1,1-dimethyl disiloxane, 1-dimethylamino- disiloxane, 1-diethylamino- disiloxane, 1-diisopropylamino- disiloxane, 1-dipropylamino- disiloxane, 1-di-n-butylamino- disiloxane, 1-di-sec-butylamino- disiloxane, 1-N-methylethylamino- disiloxane, 1-N-methylpropylamino- disiloxane, 1-N-methylbutylamino- disiloxane, 1-piperidino- disiloxane, 1-t-butylamino disiloxane, and 1-dimethylamino-1,1,5,5,5,-pentamethyl disiloxane.

[0066] Where a deposited film includes nitrogen, a nitrogen-containing reactant may be used. A nitrogen-containing reactant contains at least one nitrogen, for example, nitrogen (N_2), ammonia (NH_3), hydrazine (N_2H_4), amines (e.g., amines bearing carbon) such as methylamine (CH_5N), dimethylamine ($(CH_3)_2NH$), ethylamine ($C_2H_5NH_2$), isopropylamine (C_3H_9N), t-butylamine ($C_4H_{11}N$), di-t-butylamine ($C_8H_{19}N$), cyclopropylamine ($C_3H_5NH_2$), sec-butylamine ($C_4H_{11}N$), cyclobutylamine ($C_4H_7NH_2$), isoamylamine ($C_5H_{13}N$), 2-methylbutan-2-amine ($C_5H_{13}N$), trimethylamine (C_3H_9N), diisopropylamine ($C_6H_{15}N$), diethylisopropylamine ($C_7H_{17}N$), di-t-butylhydrazine ($C_8H_{20}N_2$), as well as aromatic containing amines such as anilines, pyridines, and benzylamines. Amines may be primary, secondary, tertiary or quaternary (for example, tetraalkylammonium compounds). A nitrogen-containing reactant can contain heteroatoms other than nitrogen, for example, hydroxylamine, t-butyloxycarbonyl amine and N-t-butyl hydroxylamine are nitrogen-containing reactants. Other examples include N_xO_y compounds such as nitrous oxide (N_2O), nitric oxide (NO), nitrogen dioxide (NO_2), dinitrogen trioxide (N_2O_3), dinitrogen tetroxide (N_2O_4) and/or dinitrogen pentoxide (N_2O_5).

Apparatus

[0067] In some embodiments, FIG. 6A is a block diagram that illustrates a substrate processing system 600 used to perform processing on a wafer 602 (also referred to as a wafer), according to some embodiments. As shown, the substrate processing system may include a chamber 634. A center column may be configured to support a pedestal for when a top surface of the wafer 602 is being processed, e.g., a film is being formed on the top surface of the wafer 602, or on the backside of the wafer 602. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead-pedestal ("ShoPed") 606. A showerhead 636 may be disposed over the ShoPed 606.

[0068] In some embodiments, the showerhead 636 may be electrically coupled to power supply 638 via a match network 640. The power supply 638 may be controlled by a control module 642, e.g., a controller. In some embodiments, power may be provided to the ShoPed 606 instead of the showerhead 636. The control module 642 may be configured to operate the substrate processing system 632 by executing process input and control for specific process recipes. Depending on whether the top surface of the wafer 602 is receiving a deposited layer or layer stack or the bottom surface of the wafer 602 is receiving a deposited layer or layer stack, the controller module 642 may set various operational inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a wafer 602, and/or the height of the wafer 602 relative to the ShoPed 606.

[0069] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the wafer 602 from the ShoPed 606 to allow an end effector (not shown) to pick the wafer and to lower the wafer 602 after being placed by the end effector. The end effector may also place the wafer 602 over spacers 644. As will be described below, the spacers 644 may be sized to provide a controlled separation of the wafer 602 between a top surface of the showerhead 636 (facing the wafer) and a top surface of the ShoPed 606 (facing the wafer).

[0070] In some embodiments, the substrate processing system 632 may further include a first gas manifold 646 that is connected to first gas sources 648, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a top surface of the wafer 602, the control module 642 may controls the delivery of first gas sources 648 via the first gas manifold 646. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the showerhead 636 that faces that wafer 602 when the wafer is resting over the pedestal.

[0071] In some embodiments, the substrate processing system 632 may further include a second gas manifold 650 that is connected to second gas sources 652, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the wafer 602, the control module 642 may control the delivery of second gas sources 652 via the second gas manifold 650. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the ShoPed 606 that faces an under surface or under side (e.g., backside) of the wafer 602 when the wafer is resting over the spacers 644. The spacers 644 may provide for a separation that optimizes deposition to the under surface of the wafer 602, while reducing deposition over the top surface of the wafer 602. In some embodiments, while deposition is targeted for the under surface of

the wafer 602, an inert gas may be flown over the top surface of the wafer 602 via the showerhead 636, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 606 to be directed to the under surface of the wafer 602.

[0072] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition and plasma treatment phases of the process. Process gases may exit the chamber 634 via an outlet. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump) may draw process gases out and maintains a suitably low pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0073] In some embodiments, a carrier ring 654 may encircle an outer region of the ShoPed 606. When the top surface of the wafer 602 is being processed, e.g., a material is being deposited thereon, the carrier ring 654 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 606. The top surface of the carrier ring 654 is generally coplanar with the top surface of the wafer 602. The carrier ring 654 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the wafer 602 sits. The carrier ring 654 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., wafer 602) in a processing chamber. The wafer edge side of the carrier ring 654 may also include a plurality of contact support structures or “tabs” which may be configured to lift the wafer 602 when the carrier ring 654 is held by the spacers 644. The carrier ring 654 may include a plurality of tabs with a quantity selected from a range to support the wafer 602 during processing. Additional details regarding embodiments of the tabs will follow.

[0074] FIG. 6B is a block diagram that illustrates another substrate processing system 632 used to perform processing on the wafer 602, according to some embodiments. In some embodiments, spider forks 656 may be used to lift and maintain the carrier ring 654 in its process height, e.g., to allow depositing in the under surface (backside) of the wafer 602. The carrier ring 654 may therefore be lifted along with the wafer 602. In some implementations, the carrier ring 654 may be rotated to another station, e.g., in a multi-station system.

[0075] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead

636) and a ShoPed 66. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination showerhead and pedestal, which enables deposition on a back-side of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal include an embedded controlled heater, wafer-lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0076] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0077] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0078] In some embodiments, the gap between the side of the wafer that does not need plasma/dep may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 (limited by the wafer bow), and such gap can be controlled. The gap may be controlled depending on process conditions.

[0079] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposit film in different areas of the back-side of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing

pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0080] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 654 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0081] Figure 7A shows a cross-sectional view of an edge region of the ShoPed 606. This view provides a cross-sectional representation of the carrier ring 654, which has a carrier ring inner radius 654a and a carrier ring outer radius 654b. In some embodiments, the carrier ring 654 includes support extensions 654c, which extend below the substantial flat surface of the carrier ring 654.

[0082] The support extensions 654c are configured to mate and sit within support surfaces defined into a top surface of the spacers 644. The support surfaces provide a complementary mating surface for the support extensions 654c, such that the carrier ring 654 is prevented from sliding or moving when supported by the spacers 644. Although three spacers are shown as spacers 644 are shown in Figure 7B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 606, and spacing is defined for supporting wafer 602 at a spaced apart relationship from a top surface of the ShoPed 606.

[0083] Further shown is that a top surface of the ShoPed 606 will include a hole pattern 606a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 606a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 606 and extend to an outer periphery of the ShoPed 606. At least one hole pattern 606a is provided at an edge hole region 607 of the hole pattern, and orifices defined in the edge hole region 607 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 606.

[0084] In one example, the angle or tilt at which the orifices in the edge hole region 607 is defined to tilt or angle away from the center of the ShoPed 106. In one embodiment, the angle

is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 607, additional distribution of process gases can be provided during backside deposition of the wafer 602. In one embodiment, the remainder orifices 606d of the hole pattern 606a are oriented substantially perpendicular to the surface of the ShoPed 106 and directed toward the underside of the wafer 602.

[0085] Figure 7B illustrates that when the wafer 602 is held by the carrier ring 654, the wafer 602 edge will sit on an edge region closer to the carrier ring inner radius 654a of the carrier ring 654. The surface of the showerhead 636 facing the top surface of the wafer 602, when positioned using spacers 644, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 602.

[0086] By way of example, the distance between the top of the wafer 602 and the surface of the showerhead 636 is preferably between about 2 mm to about .5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 636 is configured to supply an inert gas flow over the top side of the wafer 602 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 606.

[0087] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0088] Figure 8 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 800 includes a transfer module 803. The transfer module 803 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 803 is a multi-station reactor 809 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 809 may include multiple stations 811, 813, 815, and 817 that may sequentially perform operations in accordance with disclosed embodiments. Stations

may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0089] Mounted on the transfer module 803 may be one or more single or multi-station modules 807 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 800 also includes one or more wafer source modules 801, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 819 may first remove wafers from the wafer source modules 801 to loadlocks 821. A wafer transfer device (generally a robot arm unit) in the transfer module 803 moves the wafers from loadlocks 821 to and among the modules mounted on the transfer module 803.

[0090] In various embodiments, a system controller 842 is employed to control process conditions during deposition. The system controller 842 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0091] The system controller 842 may control all the activities of the deposition apparatus. The system controller 842 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 842 may be employed in some embodiments.

[0092] The depicted embodiment includes a user interface associated with the system controller 842. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0093] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by "programming." Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0094] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may be hard coded.

[0095] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0096] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 842. The signals for controlling the process are output on the analog and digital output connections of the system 800.

[0097] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0098] In some implementations, a system controller 842 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The system controller 842, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

SYSTEM CONTROLLERS

[0099] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0100] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber

in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0101] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0102] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0103] A system controller may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck.

[0104] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0105] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels,

and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

Conclusion

[0106] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. Further, while the disclosed embodiments will be described in conjunction with specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A method of reducing bow in a substrate, the method comprising:
receiving a substrate having one or more frontside layers on a frontside of the substrate,
wherein the one or more frontside layers induce a bow in the substrate;
depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;
depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type.
2. The method of claim 1, wherein the first backside layer comprises more silicon-hydrogen bonds than the second backside layer.
3. The method of claim 1, further comprising annealing the substrate, wherein a combined internal stress of the first backside layer and the second backside layer changes by less than 10% after annealing.
4. The method of claim 3, wherein annealing occurs at a temperature greater than about 700 °C.
5. The method of claim 1, wherein depositing the first backside layer and depositing the second backside layer are performed at temperatures less than about 500°C.
6. The method of claim 1, wherein a rate of depositing the first backside layer or the second backside layer is at least about 300Å per minute.
7. The method of claim 1, wherein the first type of internal stress shift is a tensile stress shift.
8. The method of claim 7, wherein the second type of internal stress shift is a compressive stress shift.

9. The method of claim 1, wherein the first backside layer and second backside layer comprise silicon nitride.

10. The method of claim 1, wherein the first backside layer and second backside layer each have an intrinsic internal stress magnitude of about 100 MPa to 1000 MPa.

11. The method of claim 1, wherein the first backside layer and second backside layer both have a tensile internal stress.

12. The method of claim 1, wherein the bow of the substrate is about 300 μ m or more.

13. The method of claim 1, wherein the bow of the substrate after depositing the first backside layer and the second backside layer is less than about 100 μ m.

14. The method of claim 1, wherein at least one of the one or more frontside layers comprises a hardmask.

15. The method of claim 1, wherein the one or more frontside layers comprise a stack of about 100 or more alternating layers.

16. The method of claim 15, wherein the stack comprises alternating oxide layers and nitride or polysilicon layers.

17. The method of claim 15, wherein the first backside layer and second backside layer have a thickness of about 0.1 μ m to about 5 μ m.

18. A substrate comprising:
one or more frontside layers on a frontside of the substrate;
a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;
a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type.

19. The substrate of claim 18, wherein, if from the one or more frontside layers are not compensated by the first backside layer, the substrate has a bow of about 300 μm or more.

20. The substrate of claim 18, wherein the first type of internal stress shift is tensile and the second type of stress shift is compressive.

21. The substrate of claim 18, wherein, if from the one or more frontside layers are not compensated by the first backside layer, the substrate has a bow of about 300 μm or more.

22. The substrate of claim 18, wherein the first backside layer and second backside layer comprise silicon nitride.

23. The substrate of claim 18, wherein the first backside layer and second backside layer have a thickness of about 0.1 μm to about 5 μm .

24. The substrate of claim 18, wherein the first backside layer comprises more silicon-hydrogen bonds than the second backside layer.

25. The substrate of claim 18, wherein a combined internal stress of the first backside layer and the second backside layer, if annealed, changes by less than 10% after annealing.

26. An apparatus for semiconductor processing, the apparatus comprising:
a process chamber; and
a controller comprising memory and processors configured for:
receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the one or more frontside layers induce a bow in the substrate;
depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;
depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type.