CLAIMS

1. An integrated structure for an optoelectronic device, the integrated structure comprising:

a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device;

a plurality of optical elements on the CMOS backplane, wherein the optical elements are based on a material system different from CMOS;

a bonding dielectric provided between the CMOS backplane and the optical elements for monolithic integration; and

a continuous common electrode layer in electrical contact with a first contact of each optical element;

wherein a second contact of each optical element is individually connected to the driver circuit in the CMOS backplane;

wherein the common electrode layer comprises an n-type epitaxial layer of the optical elements; and

wherein the n-type epitaxial layer is patterned with a micro-structure for providing a reflector disposed below the optical elements.

2. The integrated structure of claim 1, wherein the bonding dielectric is transparent.

3. The integrated structure of claims 1 or 2, wherein the reflector comprises a distributed Bragg reflector, DBR, and or a photonic crystal structure.

4. The integrated structure of any one of the preceding claims, wherein at least a portion of an electrode pad on the CMOS backplane functions as a reflector.

5. The integrated structure of any one of the preceding claims, wherein the first contacts comprise bottom contacts of the optical elements, and the second contacts comprise top contacts of the optical elements.

6. The integrated structure of any one of the preceding claims, comprising optical isolation trenches patterned between optical elements and extending at least partially through the common electrode layer to achieve optical isolation between the optical elements without breaking the electrical continuity of the common electrode layer.

7. The integrated structure of the preceding claims, comprising metal pads, lines or net patterned on the common electrode layer with direct electrical contact to enhance current spreading.

8. The integrated structure of any one of the preceding claims, further comprising electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.

9. The integrated structure of any one of the preceding claims, further comprising a micro-lens for each optical element to assist light collimation.

10. A method of fabricating an integrated structure for an optoelectronic device, the method comprising the steps of:

forming a plurality of epitaxial layers for optical elements on an epitaxial growth substrate, wherein the epitaxial layers are based on a material system different from complementary metal-oxide-semiconductor, CMOS;

providing a handle wafer;

performing a first dielectric bonding between the epitaxial growth substrate and the handle wafer such that an order of the epitaxial layers for the optical elements is reversed on the handle wafer compared to on the epitaxial growth substrate;

removing the epitaxial growth substrate to expose an n-type epitaxial layer of the epitaxial layers on the handle wafer;

processing the exposed n-type epitaxial layer for providing a common electrode layer for a first contact of each of the optical elements in the optoelectronic device;

providing a CMOS integrated circuit, IC, wafer comprising a driver circuit for the optoelectronic device; and

performing a second dielectric bonding between the handle wafer and the IC wafer such that an order of the epitaxial layers for the optical elements is reversed on the IC wafer compared to on the handle wafer;

wherein processing the exposed n-type epitaxial layer comprises pattering the exposed n-type epitaxial layer with a micro-structure for provide a reflector disposed below the optical elements.

11. The method of claim 10, further comprising patterning the epitaxial layers on the IC wafer for forming the optical elements and patterning the epitaxial layers and the common electrode layer on the IC wafer for forming contact openings.

12. The method of claim 11, further comprising pattering the epitaxial layers on the IC wafer to form optical isolation trenches.

13. The method of any one of claims 10 to 12, further comprising forming vertical interconnections between a second contact of each optical element and the driver circuit in the IC wafer.

14. The method of claim 10, further comprising patterning the epitaxial layers on the IC wafer for forming the optical elements and patterning the epitaxial layers, the common electrode layer, and a dielectric bonding layer between the optical elements and the IC wafer for forming contact openings.

15. The method of claim 14, further comprising forming a passivation layer with contact window openings on the epitaxial layers and patterning a conductive layer on the passivation layer for forming vertical interconnections between a second contact of each optical element and the driver circuit in the IC wafer.

16. The method of any one of claims 10 to 15, wherein the reflector comprises a distributed Bragg reflector, DBR, and or a photonic crystal structure.