ABSTRACT

For manufacturing a packaged semiconductor device, a lead frame (8) with an electrically insulating strip member (70) and a semiconductor chip (4) is placed in a molding unit having upper and lower dies (11a, 11b). The upper and lower dies have recessed areas (a, b) for determining a size of a cavity of the molding unit different from each other, the size of the cavity being measured in a direction perpendicular to a clamping motion direction of the dies. The lead frame is positioned so that a surface of each lead with the insulating strip member applied thereto is contacted with one (11a) of the upper and lower dies having a larger recessed area and a molding line (ML) of the molding unit intersects the insulating strip member (70). The molding unit is closed to clamp the lead frame to depress and thrust into spaces between adjacent leads that part of the strip member which is outside the molding line and to form the cavity of the molding unit. By injecting a molding material into the cavity, a molding package (2) is provided encapsulating the semiconductor chip and a portion of each lead. The packaged semiconductor device (1) has a flanged side surface (S3) with an insulating strip (7) provided between a step (SS) of the flanged side surface and intermediate portions (Li) of the leads which are between first portions (L1) of the leads encapsulated in the molding package and second portions (L2) of the

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leads protruding from the flanged side surface. An insulating filler (7') is provided in spaces between those parts of the second portions of the leads which outwardly adjoin the intermediate portions of the leads.