

Fig. 1 is a cross-sectional view of a semiconductor device. The device structure includes a top layer (AP1), a gate layer (GE), a gate insulating layer (GIS), a channel layer (150), a source/drain layer (USD1), and a bottom layer (P07, P06). The device features a series of vertical patterns (Y1, Y2, Y3, Y1', Y2', Y3') and horizontal patterns (X1, X2, X1', X2'). The bottom layer is divided into regions (P07, P06) and a central region (P07, IS2, IS1, UCH1). A coordinate system (D1, D2, D3) is shown at the bottom left.

FIG. 2

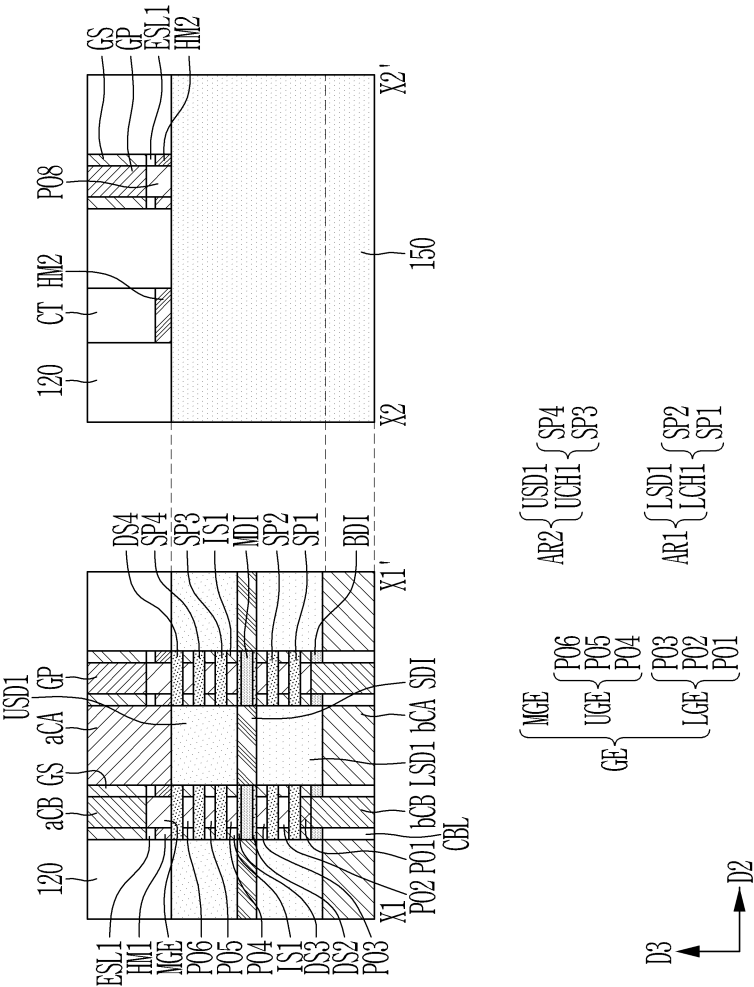


FIG. 3

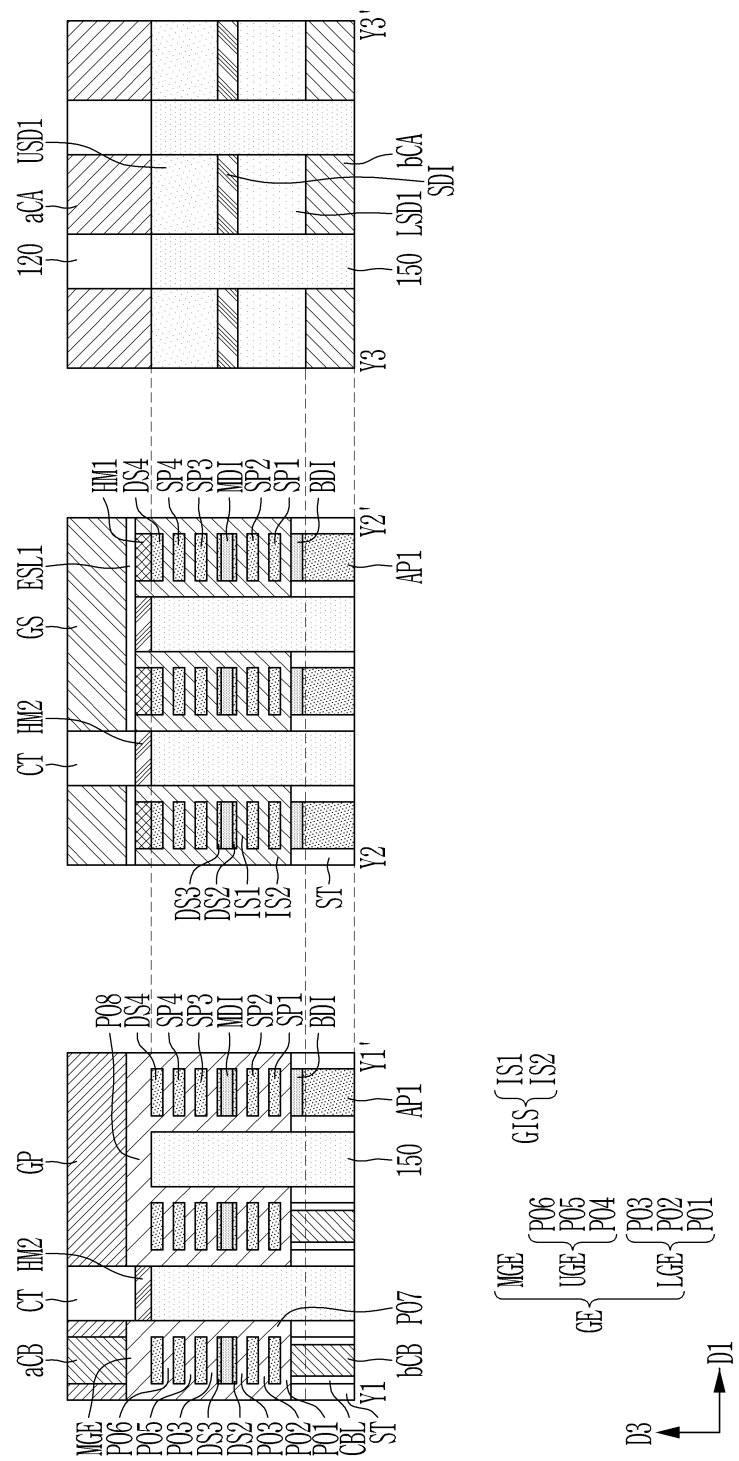


FIG. 4

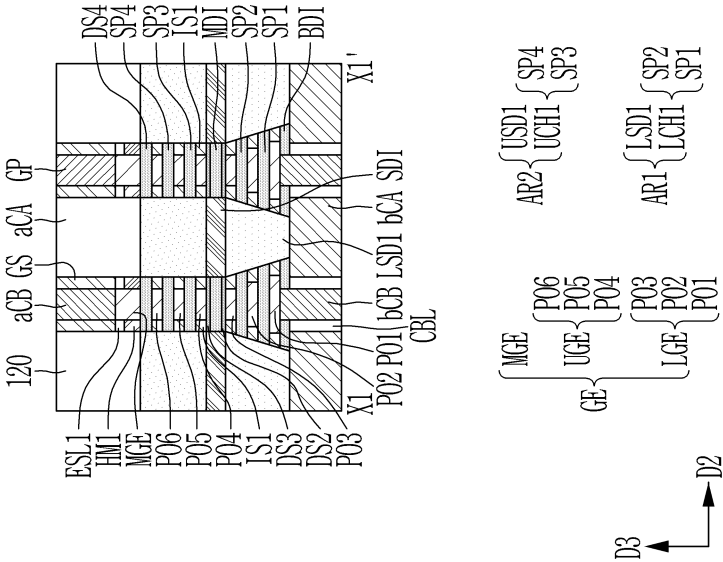


FIG. 5

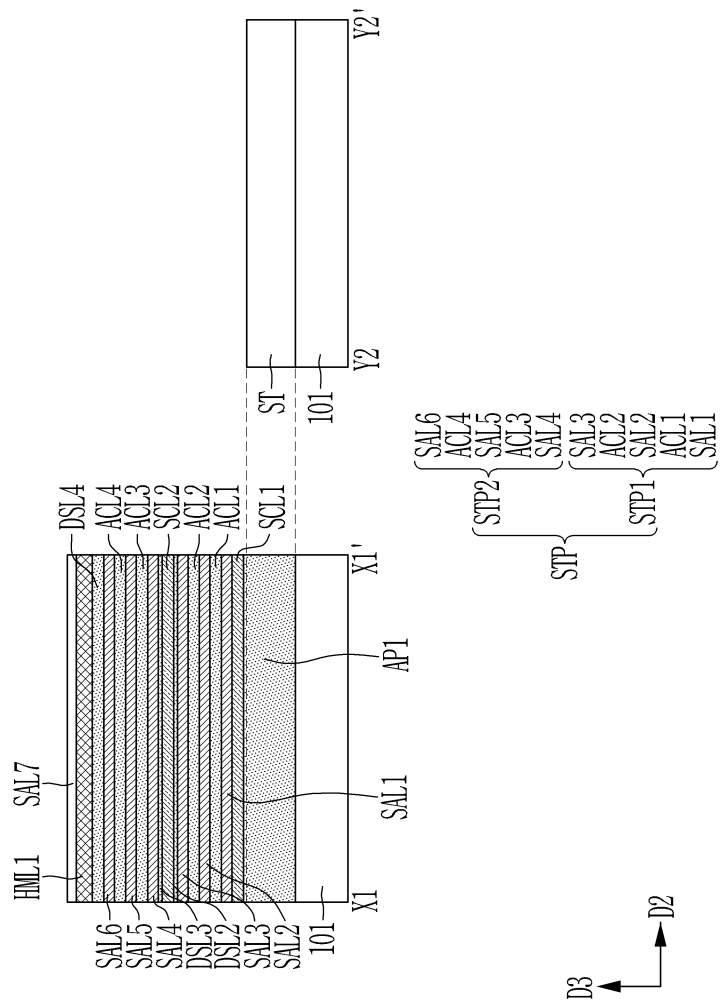


FIG. 6

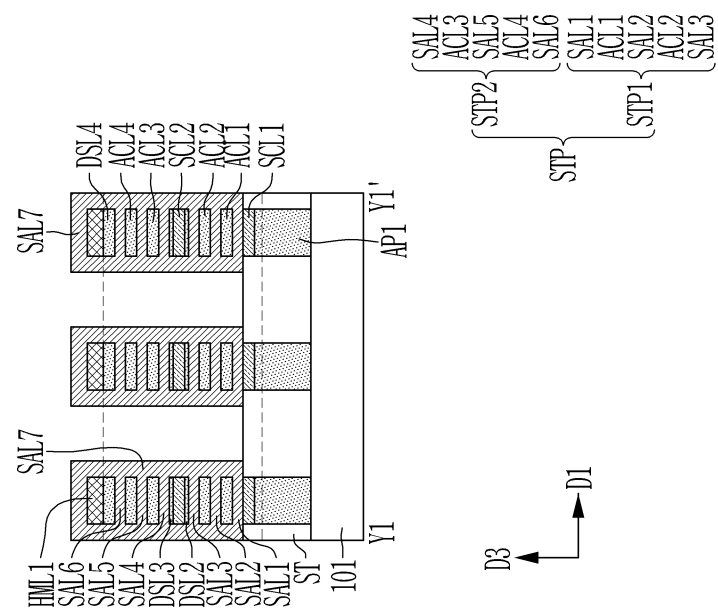


FIG. 7

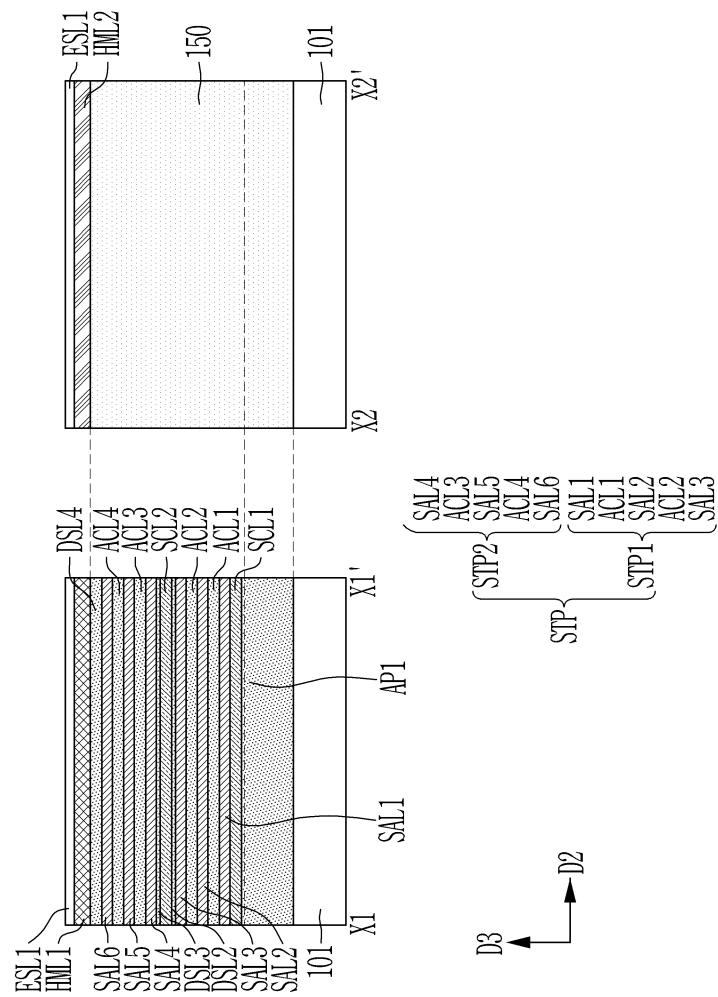


FIG. 8

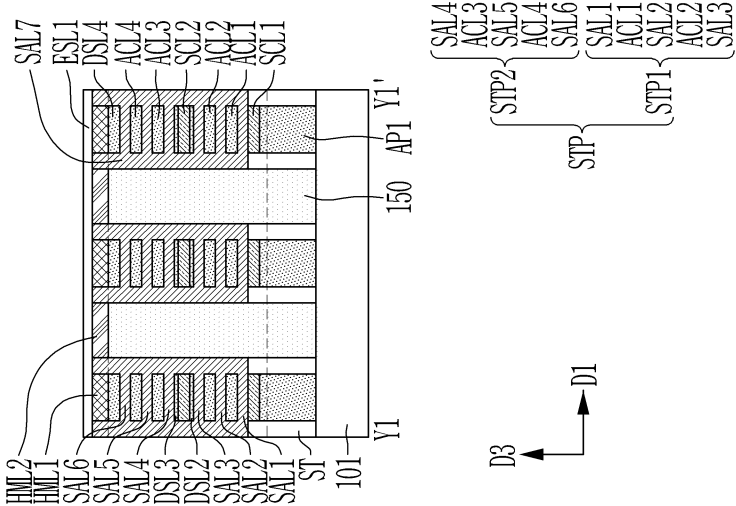


FIG. 9

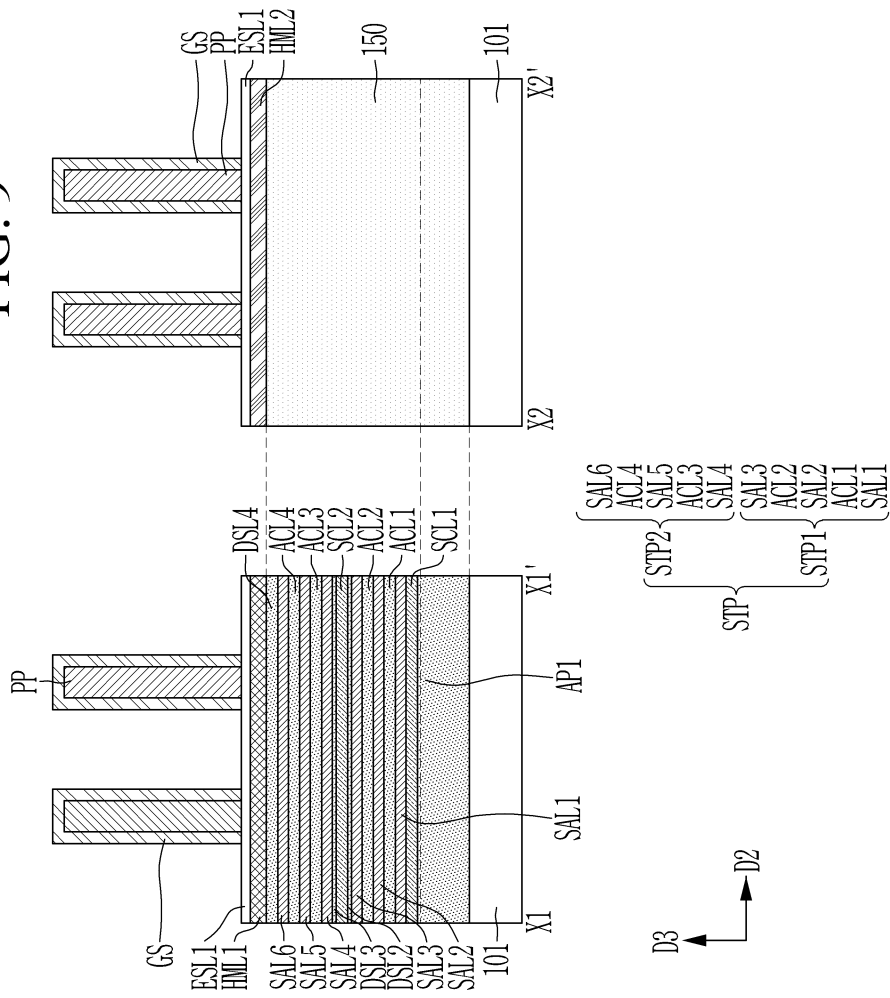


FIG. 10

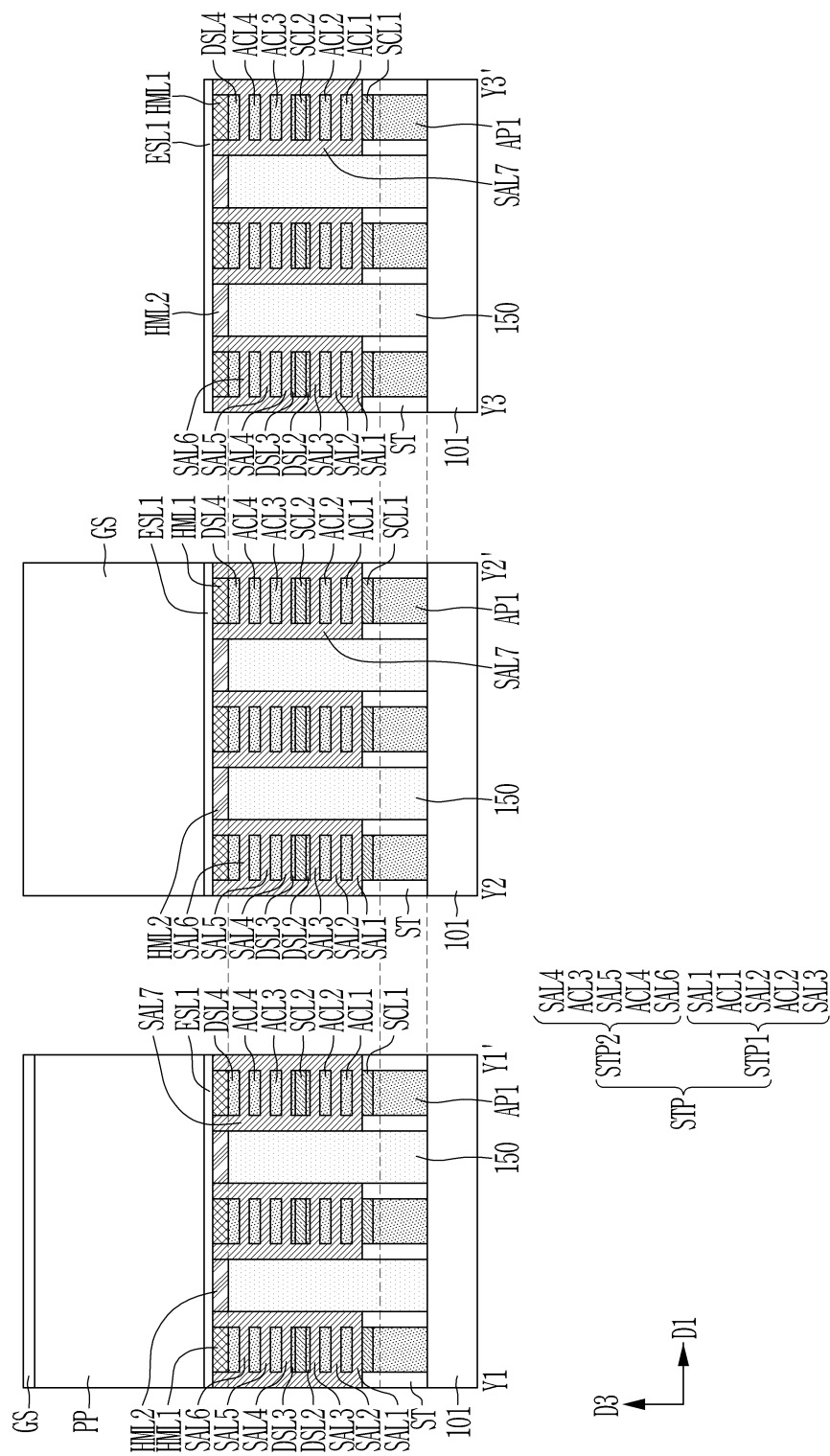


FIG. 11

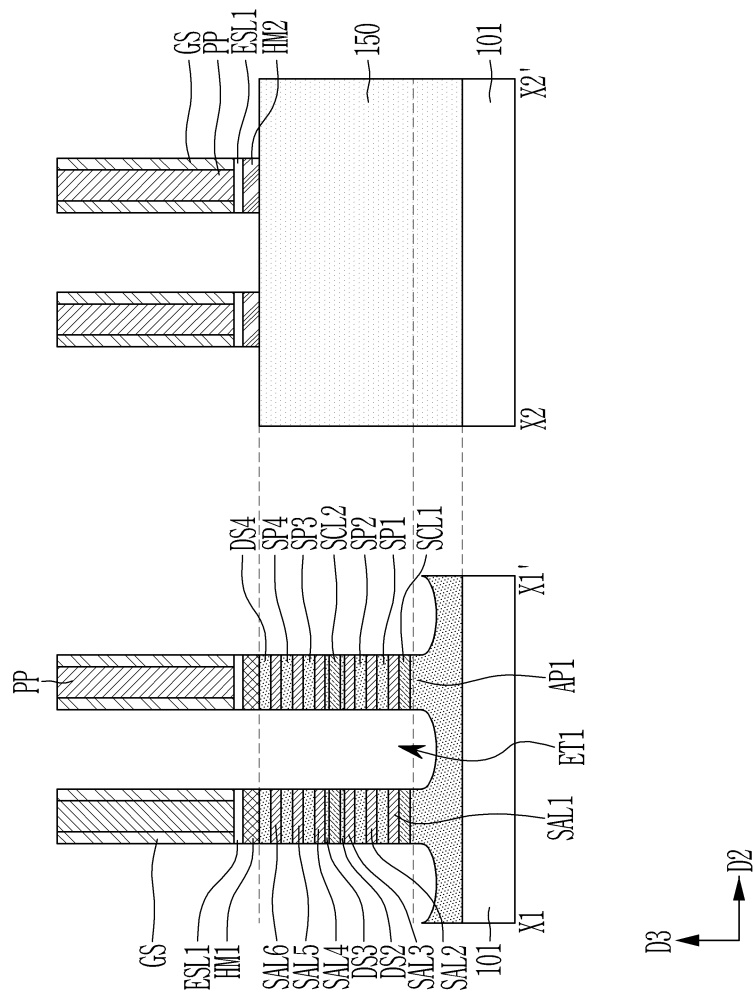


FIG. 12

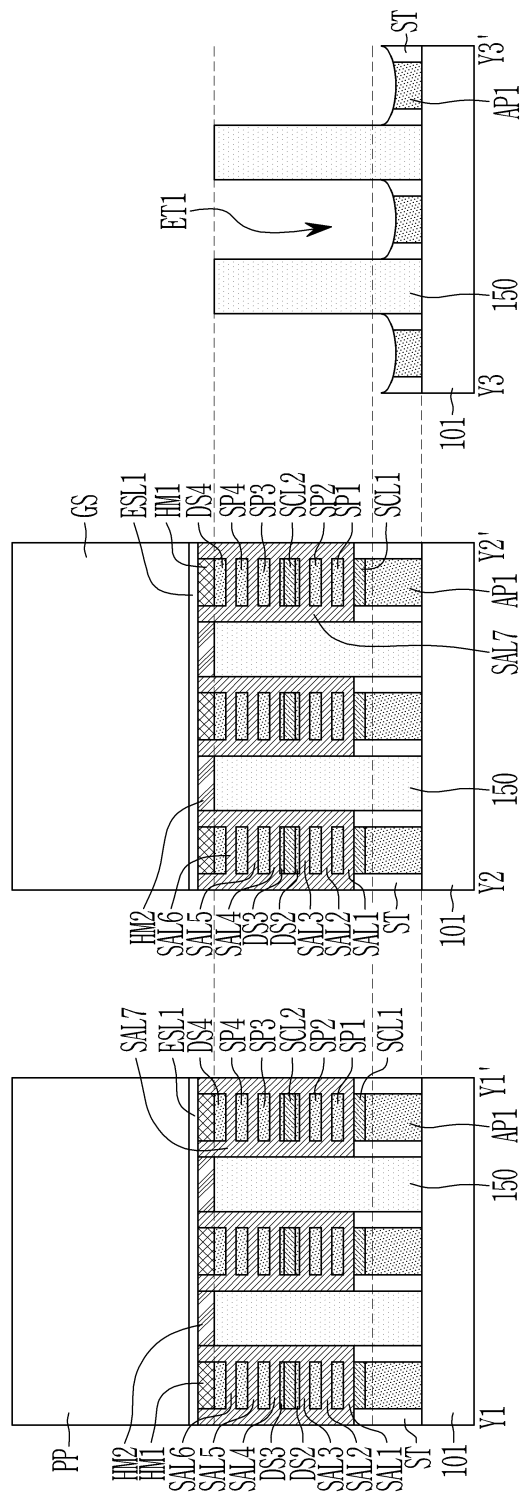




FIG. 14

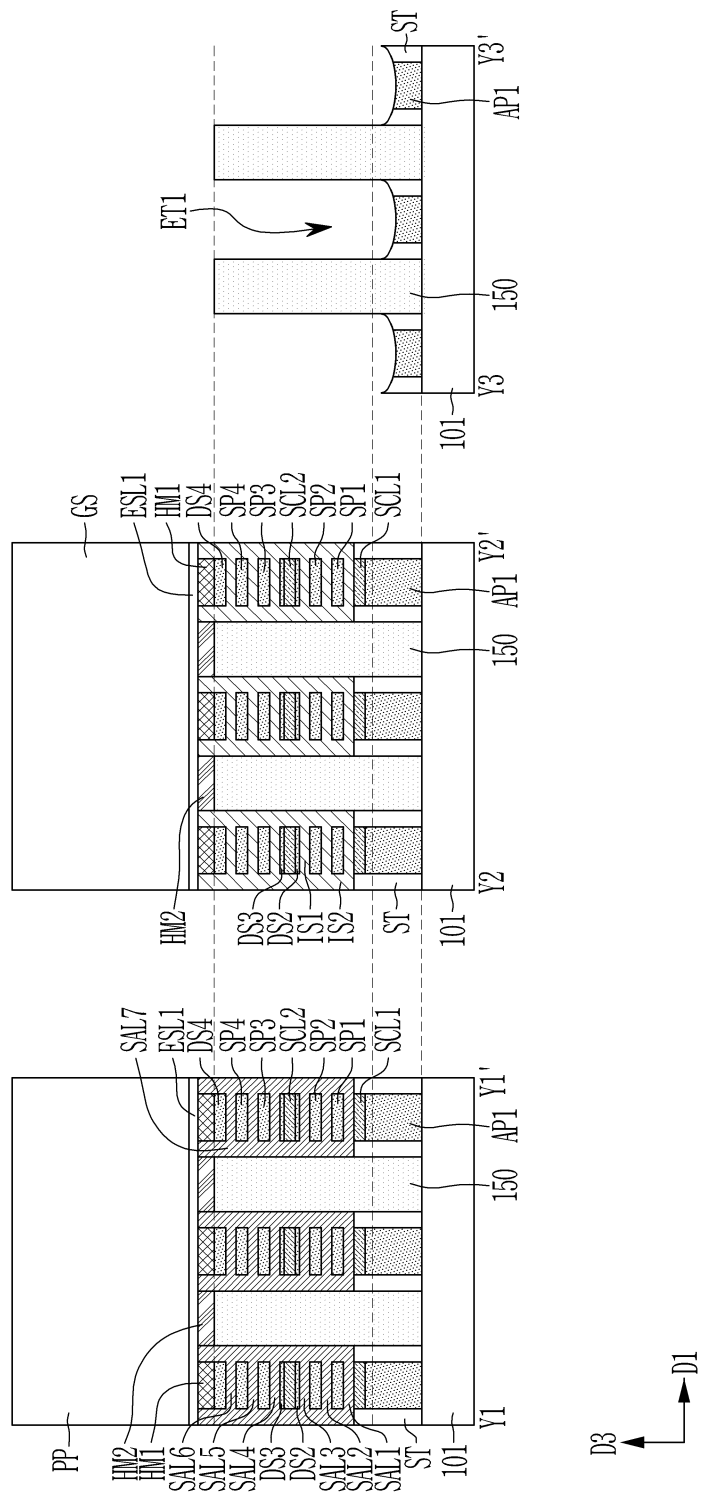


FIG. 15

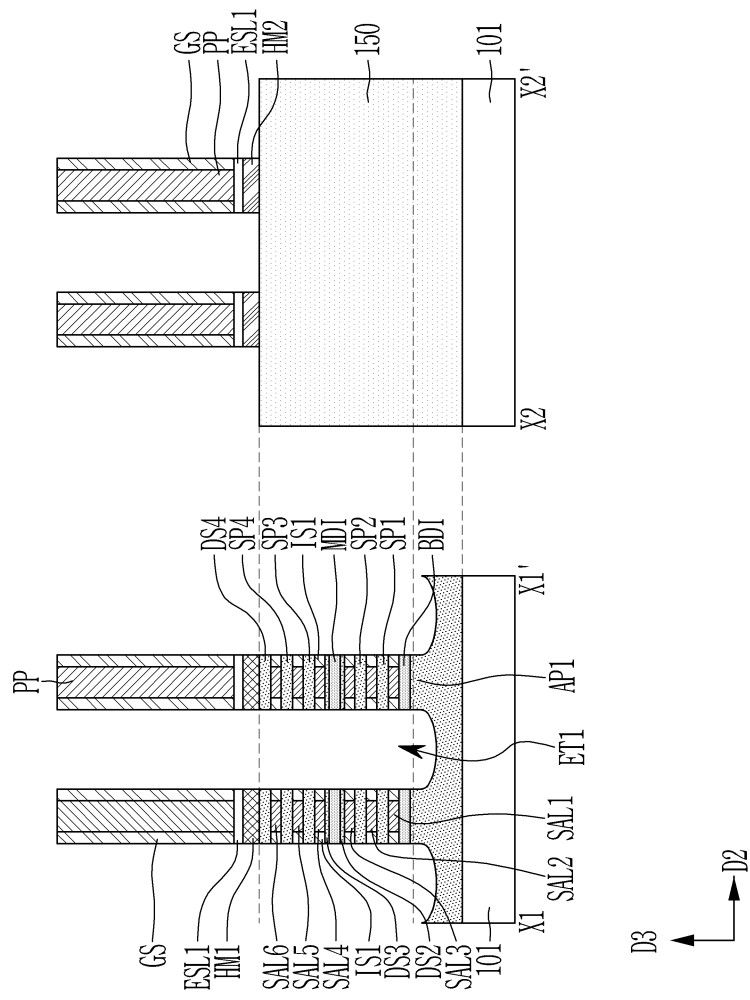


FIG. 16

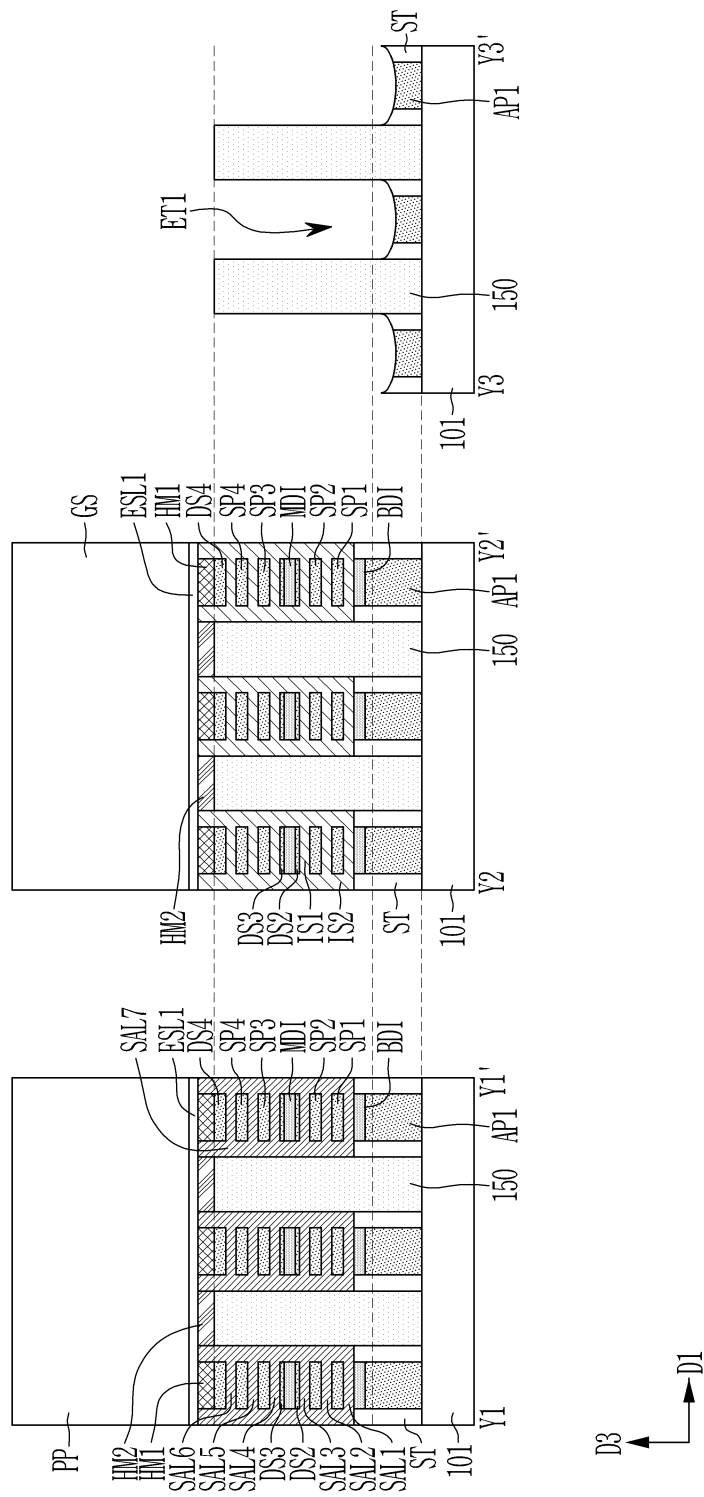


FIG. 17

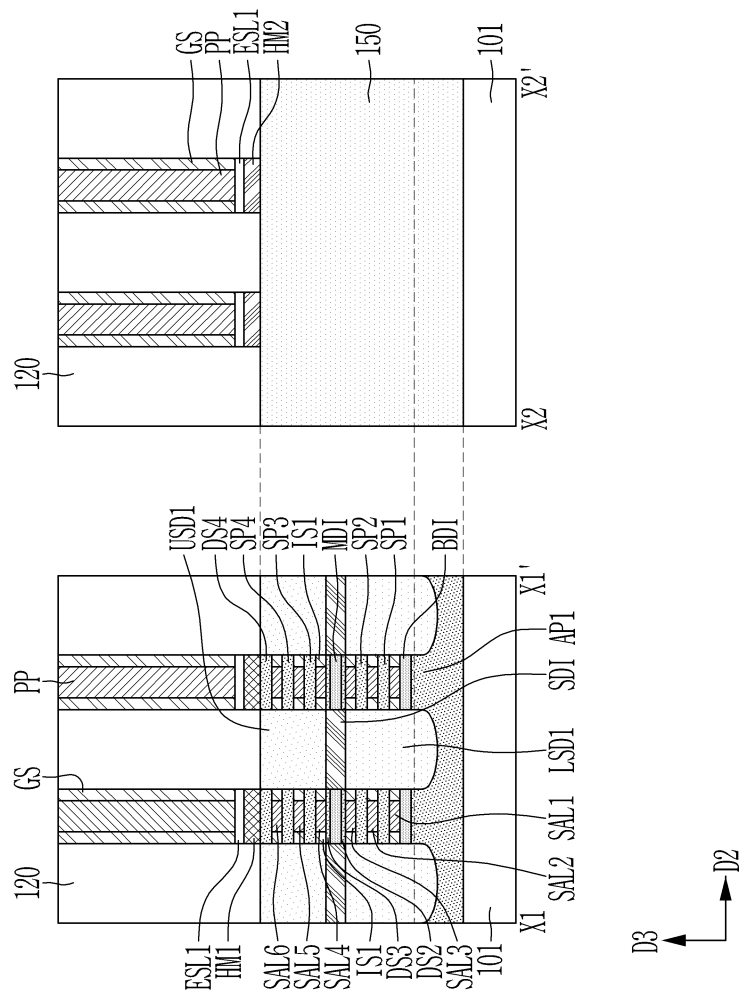


FIG. 18

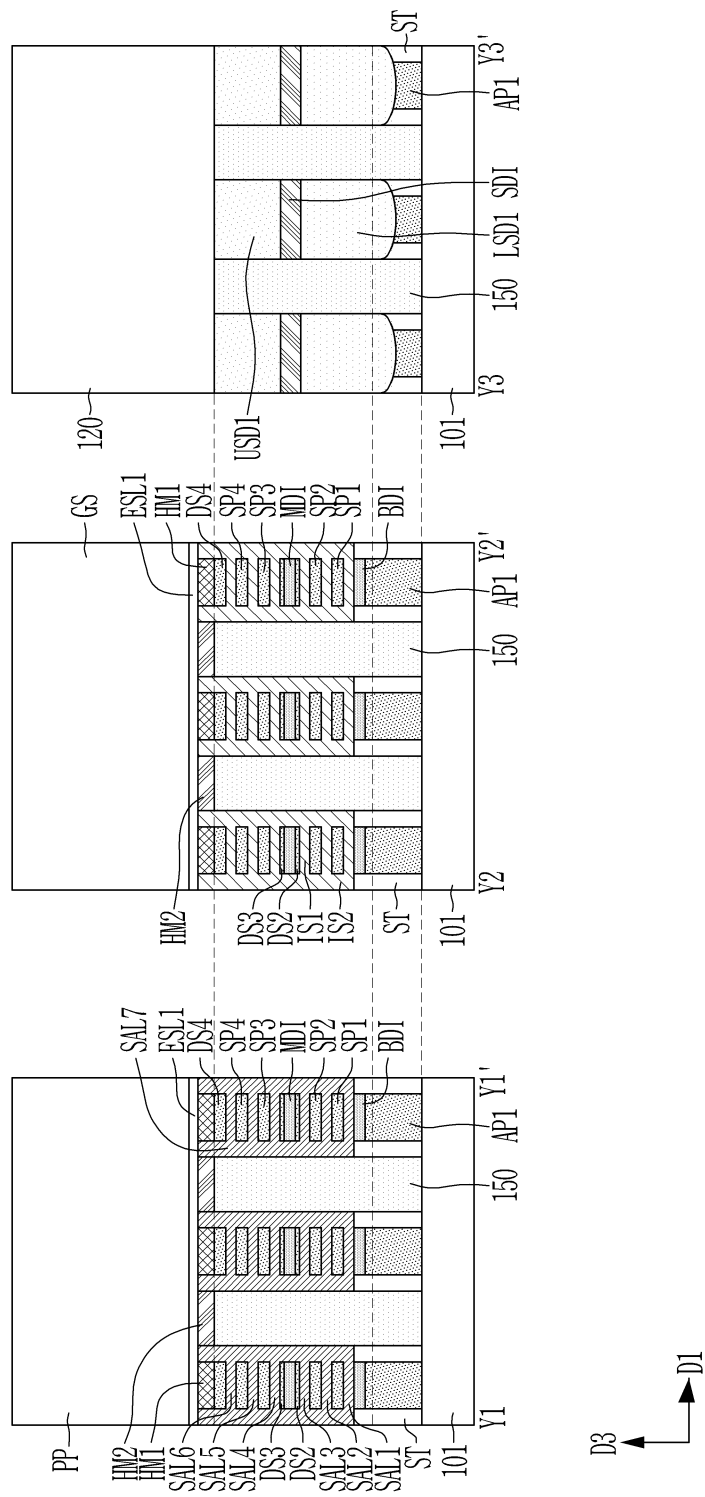


FIG. 19

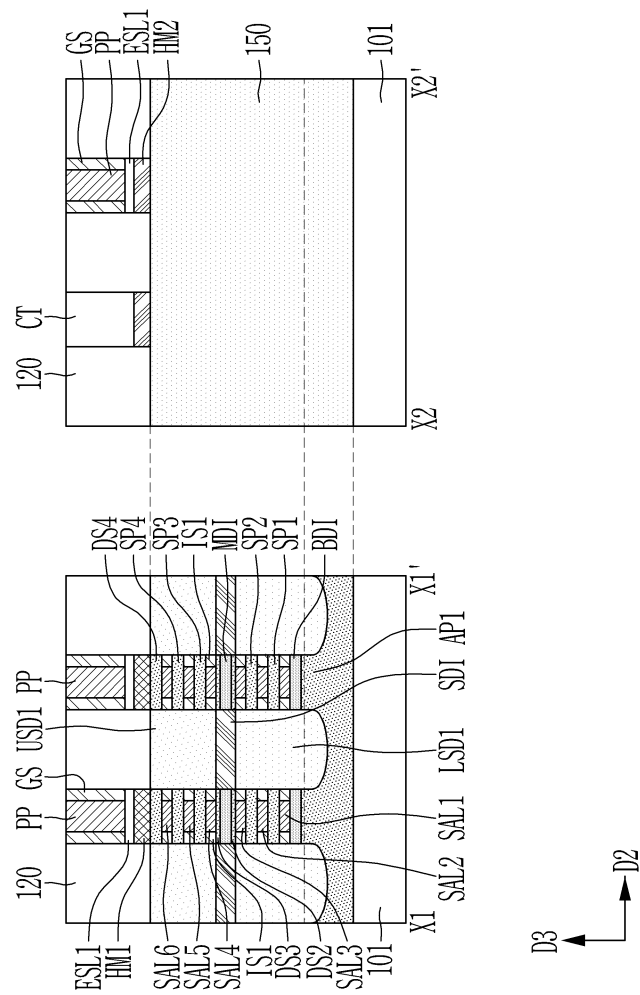


FIG. 20

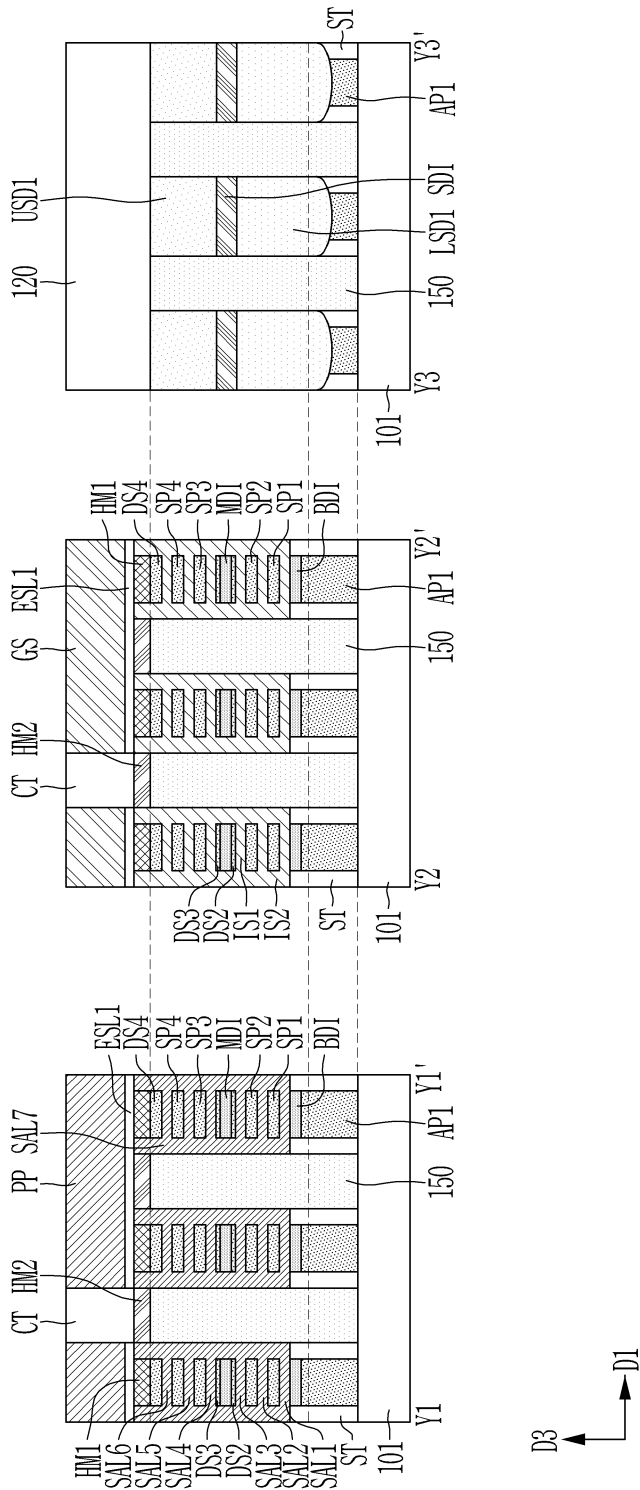


FIG. 21

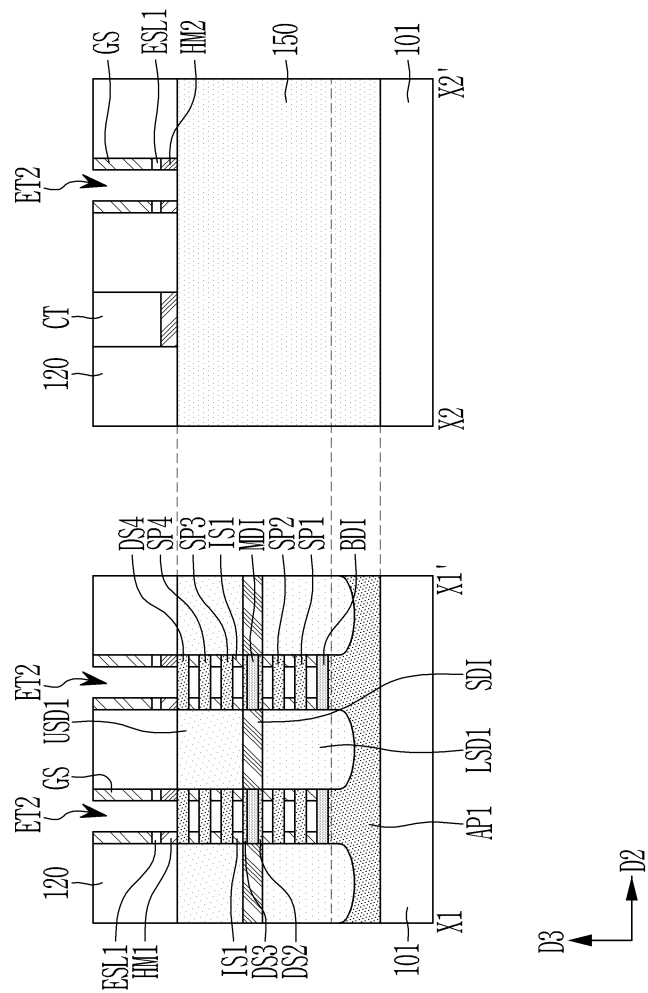


FIG. 22

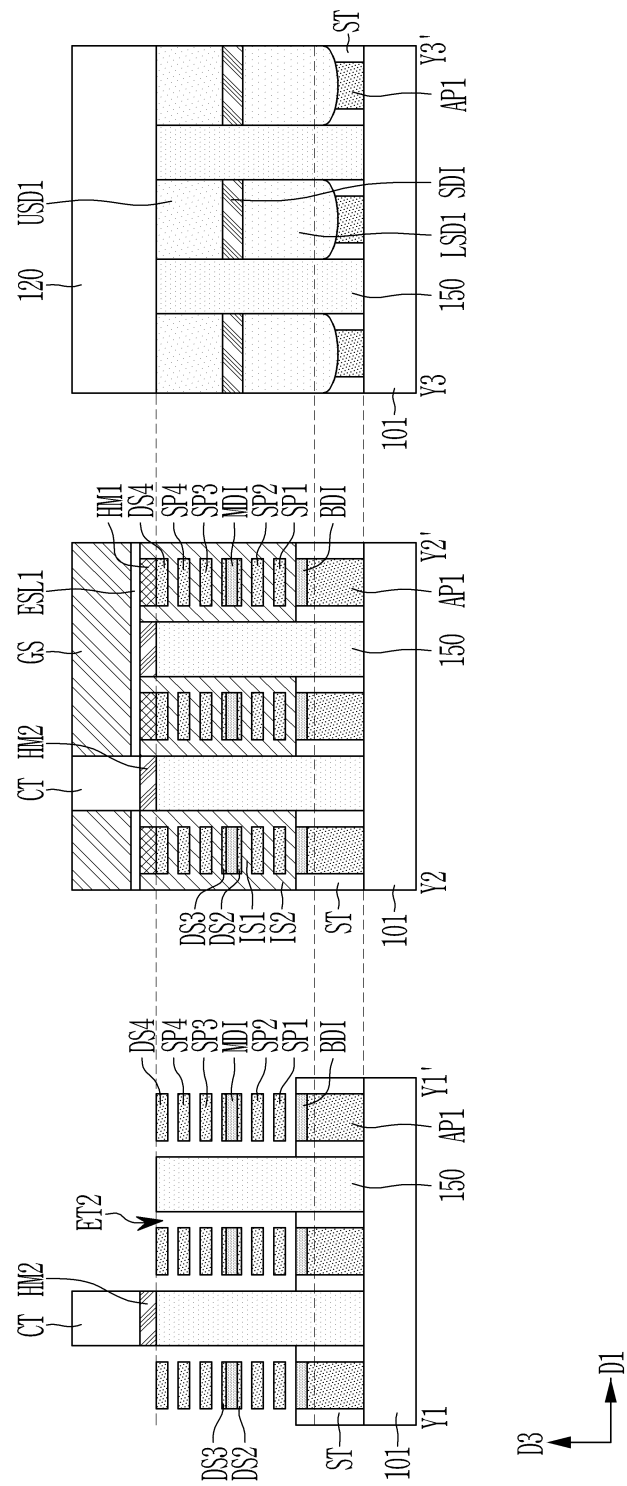


FIG. 23

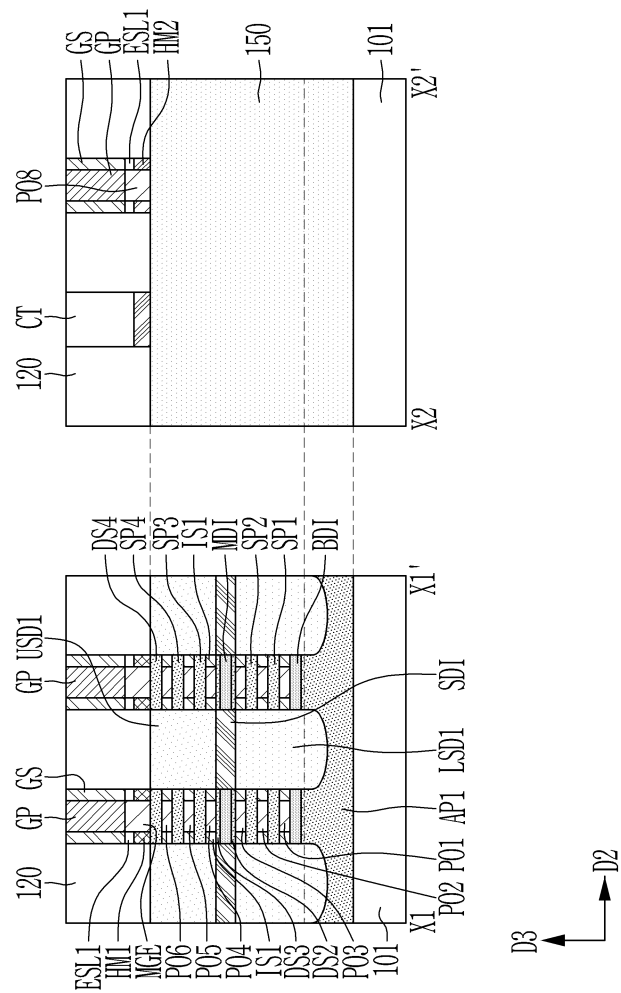


FIG. 24

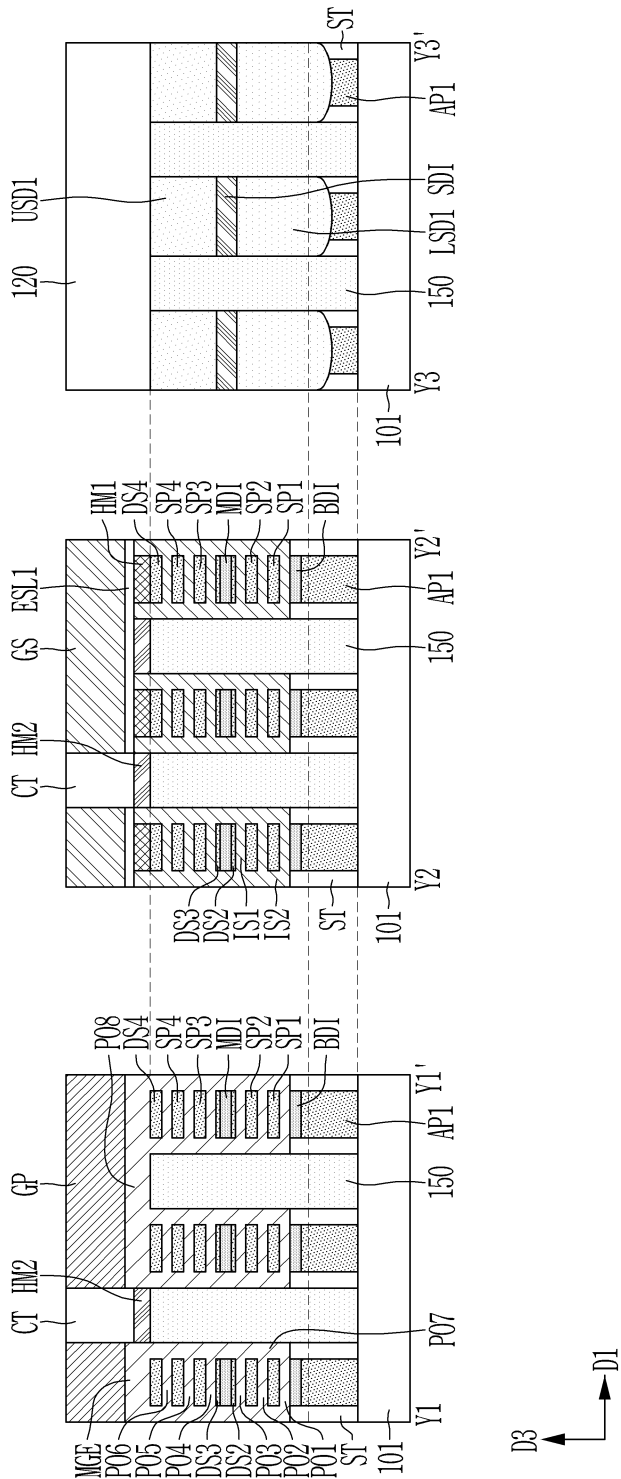


FIG. 25

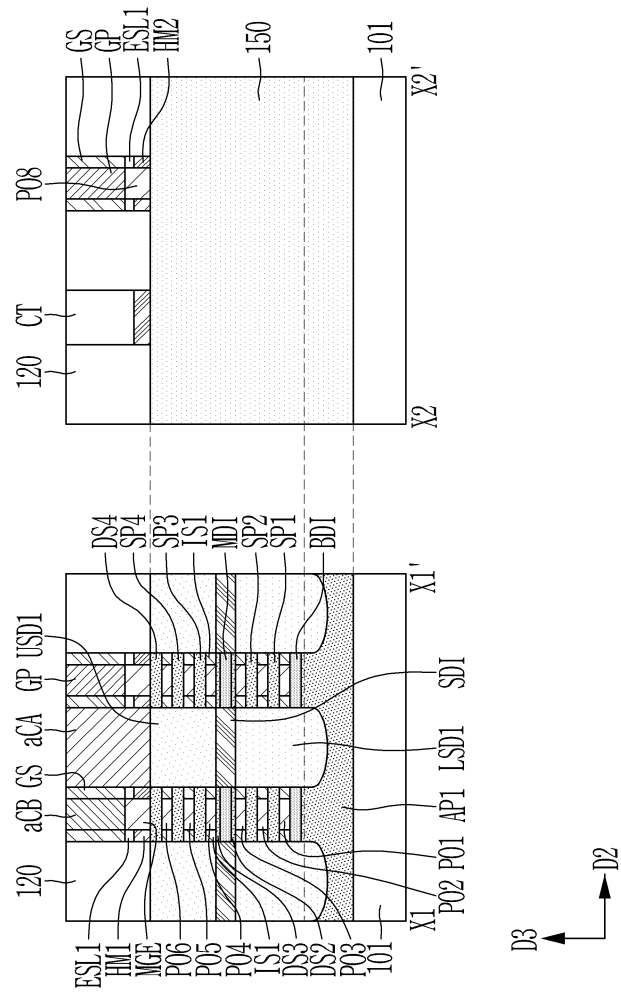


FIG. 26

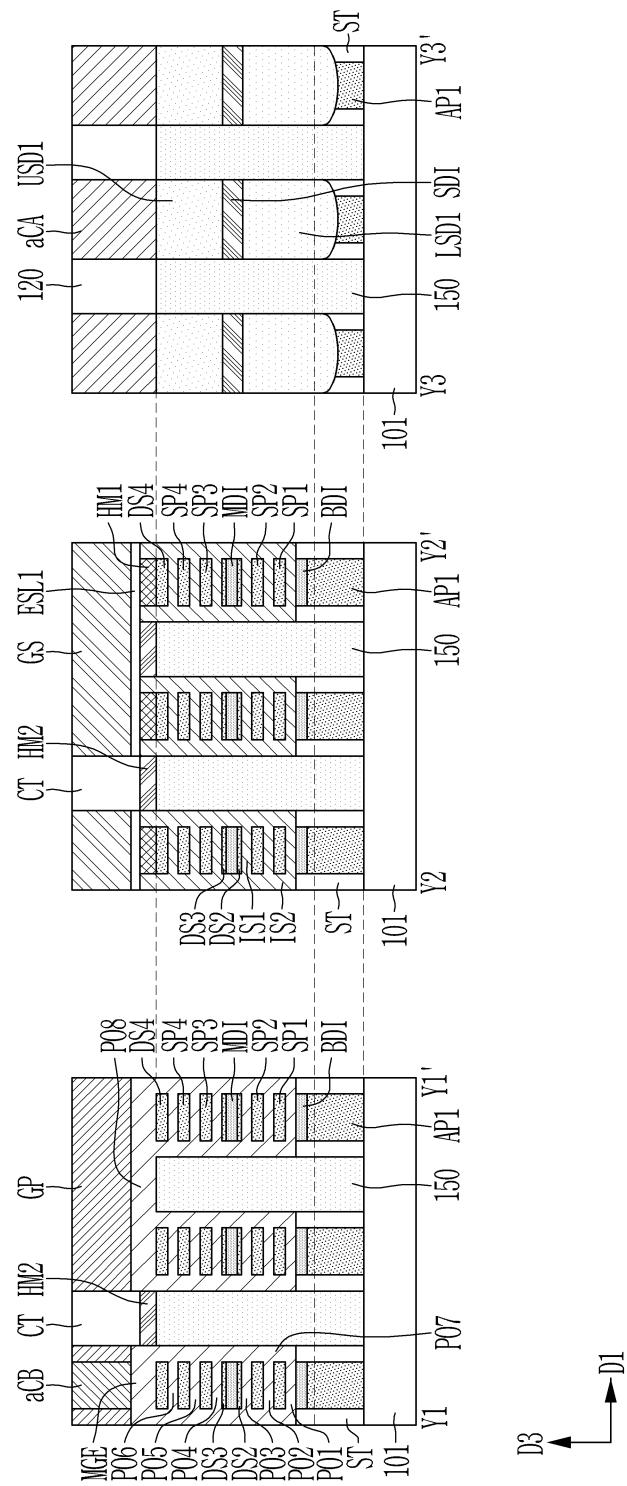


FIG. 27

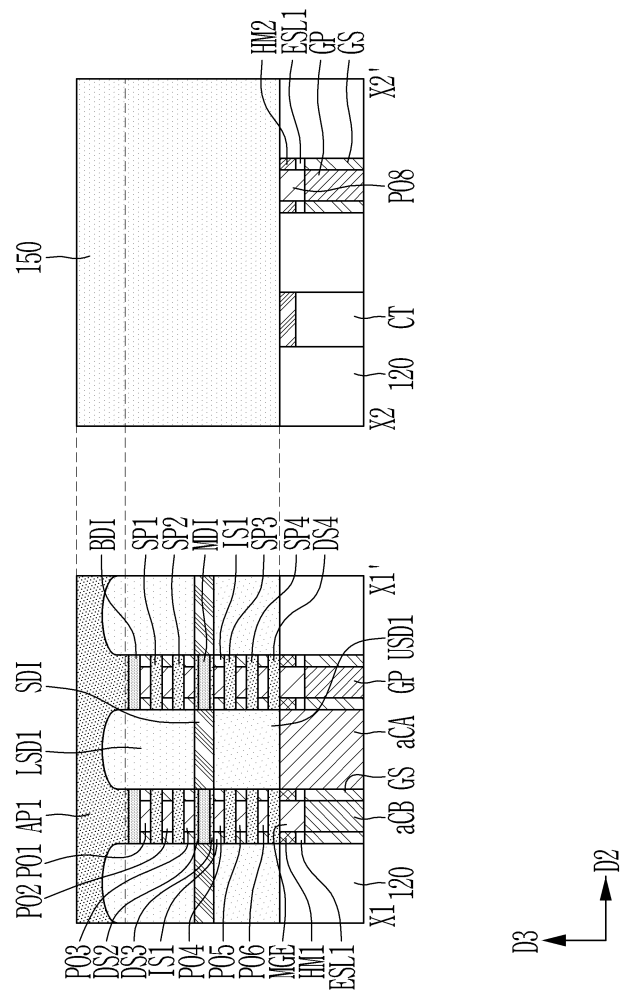


FIG. 28

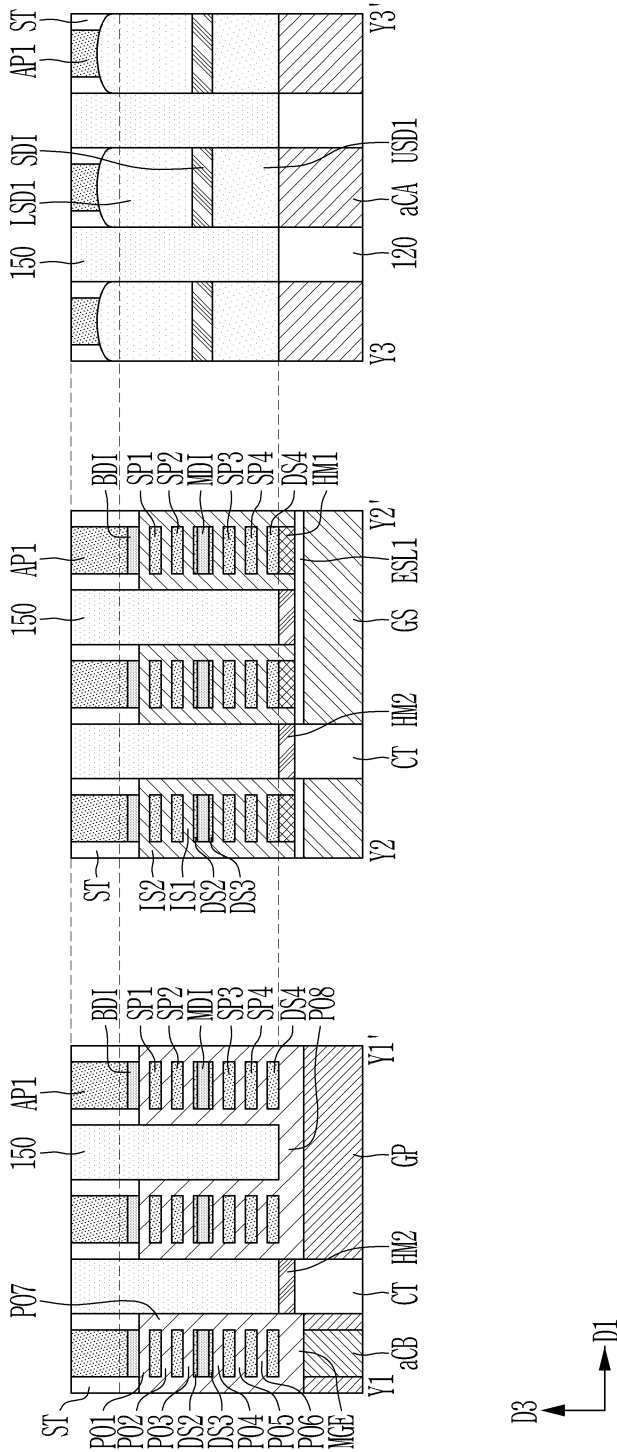


FIG. 29

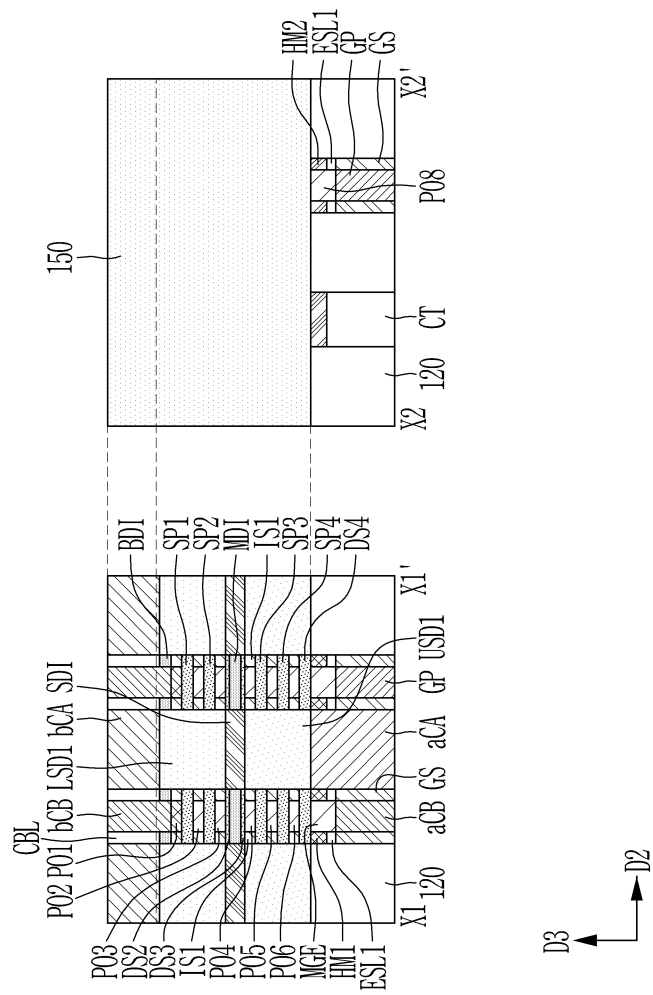


FIG. 30

