

Description

Field of Invention

This invention relates to a semiconductor transistor device structure in which current conduction involves tunneling of electrons from the emitter to the collector regions of the device.

Background of the Invention

In the art of semiconductor transistor structures, operating switching speeds of faster than about 20 picoseconds do not appear attainable either with conventional bipolar NPN (or PNP) transistor structures or with conventional unipolar N—MOS (or P—MOS) structures, even if their sizes be reduced still further, owing to natural limitations of such structures that seem fairly well understood by workers in the art. Accordingly, these workers have been seeking to devise new transistor structures that are not subject to such limitations, in order to achieve picosecond transistor switching operation.

For example, in a paper by N. Yokoyama et al. entitled "Tunneling Hot Electron Transistor Using GaAs/AlGaAs Heterojunctions," published in *Japanese Journal of Applied Physics*, Vol. 23, No. 5, pp. L311—L312 (1984), a transistor structure is taught which promises to achieve picosecond or even subpicosecond operation. That structure relies upon a relatively thick 1,000 Angstrom (100 nm) base layer composed of n-type semiconductive gallium arsenide — that is, gallium arsenide doped with significant excess donor impurities to render it conductive, particularly in the transverse directions to the high-current path. The base layer is located between an emitter layer and a collector layer — each also composed of n-type gallium arsenide — a base-emitter barrier layer composed of semiconductive undoped aluminum gallium arsenide intervening between the base and emitter layers, and an undoped base-collector barrier layer (also composed of aluminum gallium arsenide) intervening between the base and collector layers. Each such barrier layer produces a potential (electrical and/or chemical) barrier against transport of electrons therethrough. Operation depends upon tunneling of electrons from the emitter to the base layer in response to a positive voltage applied to the base layer with respect to the emitter layer. When this voltage is high enough, electrons will enter the base layer with a sufficient kinetic energy ("hot electrons") to pass through the base and be collected by the collector layer — provided that these electrons, after passing through the base layer where scattering and/or trapping reduce their kinetic energies, still have sufficient energy to surmount the base-collector barrier.

Such a transistor structure, however, suffers from a relatively low value of $\alpha = \beta/(1+\beta)$ where β is the current gain of the transistor (i.e., the ratio of the increment of collector current to an increment of base current) and α represents the "transfer ratio" — i.e., the fraction of electrons injected (as by tunneling or other phenomena) from the

emitter into the base that are collected by the collector. Specifically, the transistor has an undesirably low value of transfer ratio α of only about 0.28, whereas a desirable value of α would be at least about 0.50 and preferably much more. It is believed that this undesirably low value of α is caused by the relatively thick base layer in which the electrons passing therethrough, going from emitter to collector, lose a relatively high fraction (or even all) of their kinetic energy because of the scattering phenomena and/or trapping in the base and hence cannot then surmount the base-collector barrier. On the other hand, reducing the thickness of the base layer to reduce this loss of kinetic energy therein would result in an undesirably high transverse or "spreading" base resistance — which would increase the RC base delay, and hence would undesirably increase the transistor switching time to values equal to or greater than those conventional present-day transistors. Accordingly, it would be desirable to have a transistor structure capable of picosecond operation and having a transfer ratio α of at least about 0.50.

EP—A—0 067 276 and EP—A—0 033 876 disclose devices as set out in the preamble of claim 1. In these devices the emitter barrier layer is dimensioned and shaped so that injection of carriers into the base by tunneling. Since the base layer is thin, it is highly doped to provide high conductivity.

Summary of the Invention

With the invention as claimed the base is substantially undoped, the conductivity being provided by an inducted two-dimensional degenerate gas of charge carriers. Furthermore the height of the emitter barrier is controlled by the emitter-base voltage, so injection of charge carrier is by thermionic emission.

Brief Description of the Drawing

Fig. 1 is a cross-sectional diagram of a transistor device structure in accordance with a specific embodiment of the invention;

Figs. 2 and 3 are energy diagrams useful for explaining the operation of the transistor device shown in Fig. 1;

Fig. 4 is a cross-sectional diagram of a transistor device structure in accordance with another embodiment of the invention; and

Figs. 5—6 are cross-sectional diagrams of the transistor device structure shown in Fig. 1 during earlier stages of its manufacture.

Detailed Description

As shown in Fig. 1, a transistor device structure 100 has a semi-insulating substrate body 10 of gallium arsenide doped with chromium to provide traps in sufficient amounts to suppress electrical conduction by contaminating donor and acceptor impurities, as known in the art. Upon this substrate 10 is disposed an auxiliary collector contact layer 11 of n⁺ GaAs, i.e., gallium arsenide having strongly n-type semiconductor conduc-

tivity owing to the presence therein of significant excess donor impurities such as silicon in a concentration of typically about $2 \times 10^{18} \text{ cm}^{-3}$. The thickness of the auxiliary collector contact layer 11 is typically about 500 nm (5,000 Ångströms). Upon this auxiliary collector layer 11 is disposed a relatively thin (typically about 2 nm (20 Ångströms) protective collector contact etch-stop layer 12 of n^+ AlAs whose purpose is to delimit the penetration of the etching of the collector contact window, as more fully described below. The n^+ conductivity in this protective layer 12 is obtained by doping with impurity atoms, such as silicon, to a concentration of also about 2×10^{18} per cubic centimeter.

Upon the protective layer 12 is disposed a main collector contact layer 13 similar to the auxiliary collector contact layer 11.

Upon the main collector contact layer 13 is disposed an undoped collector barrier layer 14 of undoped $\text{Al}_a\text{Ga}_{1-a}\text{As}$, typically 150 nm (1,500 Ångströms) thick, with the atomic fraction a of aluminum in the approximate range of 0.25 to 0.45, typically about 0.34. It is desirable that the concentration of any donor and acceptor impurities be less than about 10^{16} per cubic centimeter in order not to degrade the potential barrier with a base layer 15 disposed thereupon.

The base layer 15 is undoped GaAs having a thickness of about 10 nm (100 Ångströms) and a concentration of donors and acceptors of typically less than about 10^{16} per cubic centimeter, preferably less than about 10^{15} per cubic centimeter to ensure high electron mobility of an inversion layer therein — i.e., a two-dimensional degenerate Fermi electron gas, the electrons behaving as free electrons in the directions perpendicular to the vertical (emitter to collector) direction in the drawing. The thickness of the base layer, in any event, is preferably less than about 50 nm (500 Ångströms), to minimize undesirable electron scattering effects therein, and is greater than about 5 nm (50 Ångströms), to supply sufficient space to accommodate a wave function of sufficient extent for a suitable number of quantum levels to form therein. A discussion of a two-dimensional degenerate Fermi gas is provided in a paper by T. Ando et al., entitled "Electronic Properties of Two-Dimensional Systems", published in *Reviews of Modern Physics*, Vol. 54, No. 2, pp. 437—672 (1982). An example of a two-dimensional degenerate Fermi gas in a semiconductor is an inversion layer, as known in the art of conventional MOS transistors. However, whereas the direction of the electrical current in an MOS transistor (when the transistor is "on") is in the plane of the inversion layer, in this invention the direction of the current is perpendicular to the plane of the inversion layer.

Upon the base layer 15 is disposed an emitter barrier layer 16 of undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$, typically about 150 nm (1,500 Ångströms) thick, with the atomic fraction x of aluminum varying (typically linearly) therein with vertical distances from typically about zero at the top to about 0.45 at the

bottom thereof (i.e., the interface with the base layer 15). Again, the concentrations of donor and acceptor impurities are both less than about 10^{16} per cubic centimeter in order to prevent degradation of the potential barrier at the interface with the base layer 15.

Upon the emitter barrier layer 16 is disposed a main emitter contact layer 17, which may also be called a "cap" layer, of n^+ GaAs having a thickness of typically about 20 nm (200 Ångströms) and an excess donor concentration of at least about 2×10^{18} per cubic centimeter.

Upon the main emitter contact layer 17 is disposed a protective emitter contact etch-stop layer 18 of n^+ AlAs, similar in structure to the protective collector contact etch-stop layer 12. Both of these etch stop layers are known as "spike" layers because of the spike-like shapes of the chemical compositional profile that they create.

Upon the protective emitter contact etch-stop layer 18 is disposed an auxiliary emitter contact layer 19 of n^+ GaAs (in the form of a mesa) having a thickness (height) of typically about 250 nm (2,500 Ångströms).

External electrical access to the emitter contact layer 19 is made via a first gold-germanium-silver alloy layer 21 overlaid with a gold emitter terminal layer 22. External access to the base layer 15 is made via a second gold-germanium silver alloy layer 31 overlaid with a gold base terminal layer 32. External access to the collector contact layer 11 is made via a third gold-germanium-silver alloy layer 41 overlaid with a gold collector terminal layer 42.

In order to understand the operation of the device 100, it is helpful to refer to Figs. 2 and 3. Here the zero level E_0 of electron kinetic energy (the conduction-band profile) under zero base-emitter bias voltage is designated by the solid line, and is designated in Fig. 3 by the dashed line in the case of an applied forward base-emitter voltage V_{be} . The Fermi level E_F is designated by the dot-dashed line in Figs. 2 and 3. Fig. 2 depicts the conduction-band diagram with zero bias voltage; Fig. 3 depicts it with a base-collector and a base-emitter bias voltage. For illustrative purposes, in Figs. 2 and 3 the doping in n -type contact layers 13 and 17 is nondegenerate, i.e., of order 10^{17} donor per cubic centimeter, so that the Fermi level E_F falls below E_0 instead of above E_0 as would occur in the above-described embodiment with (degenerate) doping of about 2×10^{18} donor per cubic centimeter. An applied collector-base voltage V_{cb} (Fig. 3) renders the collector positively biased with respect to the base. As a result, a degenerate Fermi gas of electrons is inducted in the base layer 15 ranging in energy between a lowest quantum level E_0 and the Fermi level E_F . Accordingly, the base layer of thickness d acts as a metal base in transverse directions.

It should be understood that in other embodiments of the invention, the degenerate Fermi gas can be present even in the absence of an applied collector voltage.

During operation, electrons thermionically emitted from the emitter (where electrons are the majority carriers) enter into the base (where they are "hot", i.e., have higher than thermal kinetic energy), pass through the base, and enter into the collector barrier layer of thickness L_2 — provided these electrons are not reflected by the barrier at the collector-base interface, of height designated in Fig. 3 by Φ_T . The barrier height for thermionic emission from the emitter into the base is controlled by the emitter-base voltage, V_{be} , as is illustrated by the dashed line in Fig. 3. The more the emitter is made negative with respect to the base (i.e., the larger the value of V_{be}), the more the number of thermal electrons that have enough energy to surmount the emitter barrier, enter into the base, and then reach the collector, hence the more the external current, as desired in transistor action.

The probability of above-barrier reflection (a quantum mechanical effect) by the barrier Φ_T of an electron of kinetic energy $E > \Phi_T$ (the lowest kinetic energy quantum level being E_0) in the base toward the collector is given by the known expression:

$$R = (n-1)^2/(n+1)^2 \quad (1)$$

where

$$n = (1 - \Phi_T/E)^{1/2} \quad (2)$$

Thus, since typically $\Phi_T = 0.2$ electron volts and $E = 0.4$ electron volts for a hot electron, it follows that typically $n = 0.7$ and $R = 0.03 = 3\%$. Thus, only about 3% of the hot electrons that enter into the base from the emitter are reflected by the collector barrier layer. This relatively low value of 3% reflection probability R should be contrasted with the undesirably relatively high reflection probability R in the case of a metal base transistor, which typically is over 50%, owing largely to the fact that in the case of a metal base the level E_0 of lowest energy is much lower, and hence Φ_T and R are much higher, than in the case of a degenerate Fermi gas in a semiconductor.

The Fermi gas of (degenerate) electrons in the semiconductor base produces a sheet resistance of about 400 Ω per square or less, which is independent of base thickness d provided d is larger than the characteristic extent of the wave function for electrons in the base. The phonon-limited mobility of electrons in the plane of the base layer is about 8,500 centimeters per volt-second at room temperature. This mobility is thus enhanced as a result of the formation of the degenerate electron gas in the relatively pure (undoped) semiconductor of the base layer. The mobility is even greater (typically over 100,000 centimeters per volt-second) at sufficiently lower temperatures, such as 77 degrees K of liquid nitrogen. An ambient low temperature of this magnitude may be desirable to reduce the thermal noise in the transistor structure. However, as far as the RC delay arising from the base

spreading resistance (the base charging time) is concerned, estimates show that even at room temperature the induced base sheet resistance is low enough so as not to interfere with the desired picosecond speed of operation.

The thickness L_2 of the collector barrier ideally is made as small as possible but not so small as to allow the collector contact layer to be short-circuited to the base, as by a short-circuit between their respective contacts for external electrical access. On the other hand, the thickness L_1 of the emitter barrier layer is advantageously sufficient to result in a desirable threshold voltage (i.e., the applied base-emitter and base-collector voltages at which the transistor structure turns on). In any event, however, this thickness L_1 should be at least about 50 nm (500 Åströms) in order to reduce undesirable depletion of the base caused by the emitter to base voltage.

Preferably the semiconductor in the base should have its conduction-band minimum located near the same electronic quasi-momentum (same point in the Brillouin zone) as does the semiconductor in the collector barrier layer. Otherwise, the transport of electrons from base to collector can be blocked in electronic momentum space. Therefore, GaAs— $Al_bGa_{1-b}As$ base-collector combination advantageously should be restricted by the condition that the atomic fraction b be less than about 0.45.

Fig. 4 illustrates an alternative embodiment in which the $Al_xGa_{1-x}As$ emitter barrier layer 16 (Fig. 2) (with x varying with distance) together with the GaAs base layer 15 are replaced by a single GaAs layer 26 having a permanent fixed negative charge sheet produced by an acceptor impurity doped (p^+) layer to form what is known as a planar-doped barrier whereby the left-hand side of the potential well is formed by a severe band-bending comprising a severe bending of the zero kinetic energy level E_0 . Advantageously, the thickness and doping level in this p^+ charge sheet is selected to be such as to produce during operation the same (or similar) desired potential well in the neighborhood of the $Al_bGa_{1-b}As$ layer 14 as in the case of the structure shown in Fig. 3. It is important that the concentration of acceptors in the charge sheet is not so high (degenerate) as to produce a conducting region thereat. Typically, the acceptor concentration is about 2×10^{18} acceptors per cubic centimeter, the thickness of this sheet is about 5 nm (50 Åströms), and the sheet is spaced from the right-hand edge of the layer 26 by a distance of about 20 nm (200 Åströms).

In an alternative embodiment, the GaAs collector layer 13 (Fig. 2) can be replaced with, for example a very highly (degenerately) doped n^+ $Al_bGa_{1-b}As$ layer 23, with b equal to typically about 0.3 in both this layer 23 and the collector barrier layer 14, and with an impurity doping concentration in layer 23 of typically about 2×10^{18} donor atoms per cubic centimeter. However, this doping need not be degenerate but may be of the order of 10^{17} donor per cubic centimeter. This

collector layer 23, because of its bandgap and n-type doping, produces a built-in electric field in the collector barrier layer 14 which induces a two-dimensional degenerate electron gas in the base even in the absence of an applied collector-base bias voltage.

Moreover, to ensure a negative threshold voltage — i.e., to ensure formation of an inversion layer in the base when the applied collector-base voltage is zero — the collector barrier layer 14 (Fig. 2) can be modulation doped with donor impurities, as known in the art, in such a manner as to result in a profile of the impurities that bend the energy bands, and hence bend the zero kinetic energy level E_0 , in particular, in a concave upward direction. For example, part of the collector barrier layer 14 of $\text{Al}_b\text{Ga}_{1-b}\text{As}$ can be doped with silicon in a uniform concentration of about 10^{18} atoms per cubic centimeter. In doing so, the region in the collector barrier layer extending for about 8 nm (80 Åströms) thereinto from the interface thereof with the base layer 15 should remain undoped. In this way, the donors, fixed in the collector barrier layer, are spatially separated from the mobile electrons in the base layer, whereby undesirable scattering, otherwise caused by the fixed donors, of mobile electrons in the base layer, (which would diminish their mobility and thus undesirably increase the base sheet resistance) is avoided. At the same time, the concave profile of the energy bands in the collector barrier layer induces an inversion layer in the base layer under the condition of zero collector-base bias.

To fabricate the transistor structure 100, the semiconductor layers 11 through 19 are successively grown epitaxially by molecular beam or other standard epitaxial processes — such as metal organic vapor deposition — upon a major surface of the substrate 10. Etching — as by means of suitable etching solutions and selective masking, as known in the art of mesa formation — followed by coating with a silicon nitride layer 20, typically 200 nm (2,000 Åströms) thick, brings the transistor being fabricated to the structure shown in Fig. 5, basically a double mesa structure with two spaced apart mesa sidewalls 51 and 52. Next, windows are opened in the contact layers 13 and 19, as by wet etching, using the layers 12 and 18, respectively, as etch stops. The lateral size of these windows can be as small as about several micrometers or less, depending upon the feature size obtainable. The portion of the silicon nitride layer 20 overlying the contact layer 19 in an immediate neighborhood of the right-hand edge of the window therein is also removed to a sufficient lateral extent for alloy contacting, again depending upon the feature size. Next, alloy layers 21, 31 and 41 of gold-germanium-silver are formed by standard procedures, to provide contacts for the emitter, base and collector, respectively. Finally, contact layers 22, 32 and 42 are formed by standard procedures, to provide electrical access to the emitter, base, and collector contact layers, respectively. The remaining

exposed top surface of the etch-stop layer 18 can then be coated with a suitable protective layer (not shown) of silicon nitride. As known in the art, external electrical circuitry (not shown) can be attached to the emitter, base, and collector terminal layers to complete an electrical circuit in which the transistor structure 100 operates as a switching device.

Although the invention has been described in detail in terms of a specific embodiment, various modifications can be made without departing from the scope of the invention as defined by the claims. For example, instead of n-type semiconductor, p-type can be used, so that the degenerate Fermi gas is of mobile holes. The potential barriers for holes, of course, are different from those for electrons. Other semiconductors can be used, such as various compound semiconductors formed by ternary and quaternary combinations of Group III with Group V elements, namely (Ga, Al, In) with (As, P, Sb), as well as combinations of Group II with Group VI elements, such as (Zn, Cd, Hg) with (S, Se, Te). Group IV elements are not ideally suited for implementation of the invention with electron-type (n-type) conduction. A major obstacle for making an n-type transistor with such Group IV heterojunction combinations as silicon and germanium lies in the fact that these materials have their conduction-band minima at different points of the Brillouin zone, thus making momentum-space reflection of electrons in germanium at the silicon interface a severe problem. However, it is feasible to implement with these materials a structure similar but complementary to that illustrated in Fig. 4 — that is, a p-type transistor with the base formed by a hole gas induced in an undoped germanium layer near the interface with a silicon layer. Silicon is a wider bandgap material than germanium, and the valence band discontinuity is known to be sufficient to confine a two-dimensional hole gas at the interface (at least at sufficiently low — e.g., liquid nitrogen — temperatures).

Also, it is feasible to use silicon or germanium substrates for subsequent growth of heteroepitaxial Group III—V compound semiconductor layers with the required energy-band profile — that is, replacing in Fig. 1 the semi-insulating GaAs substrate 10 by a Si or Ge substrate, or a Ge-coated silicon substrate. Such material combinations may be desirable for economic reasons attributable to a substantially lower cost of Si substrates.

Claims

1. A unipolar transistor comprising
 - a semiconductor emitter layer (17) having an ohmic electrical contact (21, 22) thereto,
 - a semiconductor collector layer (13) having an ohmic electrical contact (41, 42) thereto,
 - a semiconductor base layer (15) having a thickness of less than 50 nm, having an ohmic electrical contact (31, 32) thereto and situated between the emitter and collector layers.
 - a semiconductor emitter barrier layer (16)

collector layer 23, because of its bandgap and n-type doping, produces a built-in electric field in the collector barrier layer 14 which induces a two-dimensional degenerate electron gas in the base even in the absence of an applied collector-base bias voltage.

Moreover, to ensure a negative threshold voltage — i.e., to ensure formation of an inversion layer in the base when the applied collector-base voltage is zero — the collector barrier layer 14 (Fig. 2) can be modulation doped with donor impurities, as known in the art, in such a manner as to result in a profile of the impurities that bend the energy bands, and hence bend the zero kinetic energy level E_c , in particular, in a concave upward direction. For example, part of the collector barrier layer 14 of $Al_xGa_{1-x}As$ can be doped with silicon in a uniform concentration of about 10^{18} atoms per cubic centimeter. In doing so, the region in the collector barrier layer extending for about 8 nm (80 Åmströms) thereinto from the interface thereof with the base layer 15 should remain undoped. In this way, the donors, fixed in the collector barrier layer, are spatially separated from the mobile electrons in the base layer, whereby undesirable scattering, otherwise caused by the fixed donors, of mobile electrons in the base layer, (which would diminish their mobility and thus undesirably increase the base sheet resistance) is avoided. At the same time, the concave profile of the energy bands in the collector barrier layer induces an inversion layer in the base layer under the condition of zero collector-base bias.

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Also, it is feasible to use silicon or germanium substrates for subsequent growth of heteroepitaxial Group III—V compound semiconductor layers with the required energy-band profile — that is, replacing in Fig. 1 the semi-insulating GaAs substrate 10 by a Si or Ge substrate, or a Ge-coated silicon substrate. Such material combinations may be desirable for economic reasons attributable to a substantially lower cost of Si substrates.

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 - a semiconductor collector layer (13) having an ohmic electrical contact (41, 42) thereto,
 - a semiconductor base layer (15) having a thickness of less than 50 nm, having an ohmic electrical contact (31, 32) thereto and situated between the emitter and collector layers.
 - a semiconductor emitter barrier layer (16)



between and contiguous with the emitter and base layers and providing a potential barrier therebetween

and a semiconductor collector barrier layer (14) between and contiguous with the collector and base layers, forming a heterojunction with the base layer and providing a potential barrier between the collector and base layers characterized in that

the potential barrier provided by the emitter barrier layer exhibits a continuous gradual increase in the direction from the emitter layer to the base layer, whereby the height thereof is controlled by means of voltage (V_{be}) applied between the emitter and base layers,

the base layer has a dopant concentration less than 10^{16} cm^{-3} ,

and an induced two-dimensional degenerate gas of charge carriers is formed in the base layer adjacent to said heterojunction with the collector barrier layer, at least when a bias voltage (V_{cb}) is applied between said base and collector layers, said base contact forming an ohmic contact with the said charge carrier gas.

2. A transistor as claimed in claim 1 wherein the emitter barrier layer (161) is of a substantially undoped compound semiconductor of graded composition having a bandgap whose magnitude increases continuously and gradually from a lower value adjacent to the emitter layer (17) to a higher value adjacent to the base layer (15) and the emitter barrier layer forms a heterojunction with the base layer.

3. A transistor as claimed in claim 2 wherein the emitter barrier layer (16) is substantially undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ where x increases approximately linearly with distance from a lower value adjacent to the emitter layer (17) to a higher value adjacent to the base layer (15).

Patentansprüche

1. Unipolartransistor, umfassend
eine Halbleiter-Emitterschicht (17) mit einem Ohmschen, elektrischen Kontakt (21, 22) hieran,
eine Halbleiter-Kollektorschicht (13) mit einem Ohmschen, elektrischen Kontakt (41, 42) hieran,
eine weniger als 50 nm Dicke Halbleiter-Basis-schicht (15), die mit einem Ohmschen, elektrischen Kontakt (31, 32) hieran versehen und zwischen der Emitter- und der Kollektorschicht gelegen ist,

eine Halbleiter-Emitterbarrierenschicht (16), die zwischen den, sowie angrenzend an die Emitter- und Basisschichten gelegen ist und eine Potentialbarriere hierzwischen erzeugt, und

eine Halbleiter-Kollektorbarrierenschicht (14), die zwischen den, sowie angrenzend an die Kollektor- und Basisschichten gelegen ist, einen Heteroübergang mit der Basisschicht bildet und eine Potentialbarriere zwischen dadurch gekennzeichnet, daß

die durch die Emitterbarrierenschicht erzeugte Potentialbarriere eine kontinuierliche, allmähliche Zunahme in Richtung von Emitterschicht zur

Basisschicht aufweist, wodurch ihre Höhe mit Hilfe einer zwischen Emitter- und Basisschicht angelegten Spannung (V_{be}) gesteuert wird,

die Basisschicht eine Dotierstoffkonzentration von weniger als 10^{16} cm^{-3} besitzt und

ein induziertes zweidimensionales entartetes Ladungsträgergas in der Basisschicht benachbart dem Heteroübergang zur Kollektorbarrierenschicht wenigstens dann erzeugt wird, wenn eine Vorspannung (V_{cb}) zwischen Basis- und Kollektorschicht angelegt wird, wobei der Basiskontakt einen Ohmschen Kontakt mit dem Ladungsträgergas bildet.

2. Transistor nach Anspruch 1, bei dem die Emitterbarrierenschicht (16) aus einem im wesentlichen undotierten Verbindungshalbleiter mit einem Gradienten in der Zusammensetzung ist derart, daß die Größe des Bandabstandes kontinuierlich und allmählich von einem kleineren Wert benachbart der Emitterschicht (17) auf einen größeren Wert benachbart der Basisschicht (15) zunimmt, und die Emitterbarrierenschicht einen Heteroübergang mit der Basisschicht bildet.

3. Transistor nach Anspruch 2, bei dem die Emitterbarrierenschicht (16) im wesentlichen undotiertes $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ist, wobei x mit dem Abstand angenähert linear von einem niedrigeren Wert benachbart der Emitterschicht (17) auf einen höheren Wert benachbart der Basisschicht (15) zunimmt.

Revendications

1. Un transistor unipolaire comprenant:

une couche d'émetteur en semiconducteur (17) sur laquelle est formé un contact électrique ohmique (21, 22),

une couche de collecteur en semiconducteur (13) sur laquelle est formé un contact électrique ohmique (41, 42),

une couche de base en semiconducteur (15) ayant une épaisseur inférieure à 50 nm, sur laquelle est formé un contact électrique ohmique (31, 32) et qui est située entre les couches d'émetteur et de collecteur,

une couche de barrière d'émetteur en semiconducteur (16) entre les couches de base et d'émetteur, et contiguë à ces dernières et établissant une barrière de potentiel entre elles,

et une couche de barrière de collecteur en semiconducteur (14) entre les couches de collecteur et de base, et contiguë à ces dernières, formant une hétérojonction avec la couche de base et établissant une barrière de potentiel entre les couches de collecteur et de base, caractérisé en ce que

la barrière de potentiel qui est établie par la couche de barrière d'émetteur présente une augmentation progressive continue dans la direction allant de la couche d'émetteur vers la couche de base, grâce à quoi sa hauteur est commandée au moyen de la tension (V_{be}) qui est appliquée entre les couches d'émetteur et de base,

la couche de base a une concentration de dopant inférieure à 10^{16} cm^{-3} ,



et un gaz de porteurs de charge, qui est un gaz dégénéré bidimensionnel induit, est formé dans la couche de base en position adjacente à l'hétérojonction avec la couche de barrière de collecteur, au moins lorsqu'une tension de polarisation (V_{bb}) est appliquée entre les couches de base et de collecteur, le contact de base formant un contact ohmique avec le gaz porteur de charges précité.

2. Un transistor selon la revendication 1, dans lequel la couche de barrière d'émetteur (16) est un semiconducteur composé pratiquement non dopé, dont la composition varie progressivement, ayant une bande interdite dont la valeur augmente continuellement et progressivement depuis une valeur inférieure dans une position

adjacente à la couche d'émetteur (17), jusqu'à une valeur supérieure dans une position adjacente à la couche de base (15), et la couche de barrière d'émetteur forme une hétérojonction avec la couche de base.

3. Un transistor selon la revendication 2, dans lequel la couche de barrière d'émetteur (16) consiste en $Al_xGa_{1-x}As$ pratiquement non dopé, dans laquelle x augmente de façon approximativement linéaire en fonction de la distance, depuis une valeur inférieure dans une position adjacente à la couche d'émetteur (17), jusqu'à une valeur supérieure dans une position adjacente à la couche de base (15).

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