

Abstract of the Disclosure**THE TRACEBACK-PERFORMING APPARATUS IN VITERBI DECODER**

The traceback-performing apparatus including a first storing portion for receiving and storing new path metric values and minimum path metric value so that the first input value is output later and the later input value is output first, a first trace logic portion for receiving outputs of the first storing portion and the minimum path metric value and generating a first state which is the next state to be traced, a second storing portion for receiving and storing the output of the first storing portion so that the first input value is output first and the later input value later, a second trace logic portion for receiving the output of the second storing portion and the first state and generating a second state which is the next state to be traced, and a third storing portion for receiving and storing the second state so that the first input value is output later and the later input value is output first so as to find the decoded bits.

Therefore, cost is saved in embodying the Viterbi decoder in a VLSI by totally reducing a chip area and making the embodiment easy, since an address-generating for a memory is simple and a global interconnection does not exist.

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This Sheet Has Been Replaced

