METHOD TO LOWER WORK FUNCTION OF GATE ELECTRODE THROUGH Ge IMPLANTATION

ABSTRACT

A method for forming selective P type and N type gates is described. A gate oxide layer is grown overlying a semiconductor substrate. A polysilicon layer is deposited overlying the gate oxide layer. Germanium ions are implanted into a portion of the polysilicon layer not covered by a mask to form a polysilicon-germanium layer. The polysilicon layer and the polysilicon-germanium layer are patterned to form NMOS polysilicon gates and PMOS polysilicon-germanium gates. In an alternative, nitrogen ions are implanted into the polysilicon-germanium layer and the gates are annealed after patterning to redistribute the germanium ions throughout the polysilicon-germanium layer. In a second alternative, germanium ions are implanted into a first thin polysilicon layer, then a second polysilicon layer is deposited to achieve the total polysilicon layer thickness before patterning the gates.

Fig. 17