

PATENT SPECIFICATION

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(54) A DYNAMIC DISPLAY SYSTEM

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- (71) We, HITACHI LIMITED of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—
- 10 The present invention relates to a dynamic display system for electronic desk-top calculators, and more specifically to a pulse lighting display system for lighting display devices in a time-sharing manner.
- 15 Generally display systems are classified into static and dynamic display types. For electronic desk-top calculators the classic static systems are being replaced by dynamic display ones which permit a reduction in the number of decoder circuits and drive circuits, that the static type requires for each digit to be handled. The dynamic display system, which takes advantage of the after-image effect of the human eyes, sequentially lights a plurality of display devices with pulses in a time-sharing manner, and thereby reducing the overall number of decoder and drive circuits to a number which is just sufficient for one digit. For this purpose it is important to establish accurate synchronism between the timing pulses (timing signals) for energizing a common electrode of a display device, and the display signals for pulse energizing desired segment electrodes of the display device. Actually, however, the lag of display signals due to their passage through the decoder and drive circuits, and the lag of timing signals due to their passage through buffer circuits, have presented the problem of imperfect synchronism between the display and timing signals. The imperfect synchronism in turn causes flicker (double lighting) of the display devices. The flicker also stems from overlapping of the display signals.
- 45 According to the present invention there is provided a dynamic display system operating in a time-sharing manner, comprising a plurality of display devices; means for applying consecutive timing signals to the respec-

tive display devices for time sharing energization thereof; means for selectively applying display signals to selected display devices to actuate the display devices in selected combinations, said display devices being energized only upon coincident receipt of a timing signal and a display signal; blanking means for generating blanking signals having a pulse width sufficient to cover the border time between adjacent display or timing signals; and gating means for gating said blanking signals with said display signals or said timing signals so as to prevent application of said display signals or said timing signals during the period of the blanking signals.

The present invention will now be described in greater detail, by way of example, with reference to the accompanying drawings, wherein:—

Figure 1 is a block diagram of a preferred form of dynamic display system; and

Figures 2 and 3 are waveforms plotted to a base of time which assist in the explanation of the circuit shown in Figure 1.

Referring to Figure 1, the dynamic display system includes a shift register Rs and a register R for four bits (for one decimal digit) to which the output from the shift register Rs is supplied. The contents (binary-coded decimal digits, i.e. four-bit serial signals) of the register R are fed back in sequence to the input of the dynamic shift register Rs. The display system also includes a memory circuit Mo to which the bit outputs from the register R are supplied. The memory circuit Mo reads the four-bit serial signals, which sequentially circulate in the register R and the shift register, with the timing of digit pulses Dp (see Figure 2g) having a cycle period corresponding to the length of the four-bit signal. The memory circuit Mo is combined with inverters IN1—IN4 to form a memory circuit M. The output from the memory circuit M is supplied to a decimal decoder Dc1 in which binary numbers are converted into decimal ones. A segment decoder Dc2 is provided for converting the output signals from the decimal decoder Dc1, into signals for energizing certain segment electrodes of dis-

play devices for displaying certain numerals. The decimal decoder Dc1 and the segment decoder Dc2 constitute a decoder circuit Dc. A blanking circuit Bc is provided for generating a signal BL for controlling the display signals from the decoder circuit Dc. The blanking circuit Bc produces the blanking signal BL by causing a bit signal Bt4 from a ring counter to be delayed by half a bit by an insulated-gate field effect transistor T1 and allowing an inverter circuit IN5 consisting of insulated-gate field effect transistors T2 and T3 to generate an inverted version of the delayed bit signal. The ring counter includes three flip-flops F1 to F3 and a NAND gate NA1 connected in conventional manner. Control AND gates A1 to Am are arranged to receive the blanking signal BL and output signals from the decoder Dc. A drive circuit Dr is provided for driving display devices to which output signals from the AND gates A1 to Am are supplied. Where Nixie tubes are employed as display devices, the segment decoder Dc2 is not required because a Nixie tube has cathode electrodes indicating decimal numbers which can be energized by the output of decimal decoder Dc1. The system also includes a display unit Dp consisting of positional display devices Dp1 to Dpn for receiving outputs from the drive circuit Dr, the symbol Dpn signifying the display device in the n-th position. The respective display units Dp1 to Dpn are provided with input terminals D1 to Dn which receive respective timing signals Dt1—Dtn.

Referring to Figure 2, various timing pulses which are used in the system shown in Figure 1 will now be explained.

Clock pulses Cp1 and Cp2 which take the form of shift pulses are staggered in phase relation to each other and are used to drive the registers Rs and R. Bit signals Bt1 to Bt4 are generated by the ring counter using the clock pulses Cp1 and Cp2 and are synchronized with the clock pulse Cp2. They are used in a separate circuit wherein parallel binary signals from an encoder (not shown) are converted into series ones, and therefore the first to fourth bits in each position of binary-coded decimal signals that circulate through the registers Rs and R are synchronized, respectively, with the bit pulses Bt1 to Bt4. A digit pulse Dp can be synthesized from the clock pulse Cp and bit signal Bt4. Letting Dpm, Cp1m and Bt4m be the respective logic representations of the digit pulse Dp, the clock pulse Cp1 and the bit signal Bt4 then

$$Dpm = \overline{Cp1m} \cdot Bt4m$$

Display timing signals Dt1 to Dtn have a pulse width equal to the sum of pulse widths of the bit signals Bt1 to Bt4 or equal to a decimal position of a binary-coded decimal

signal. The pulse cycle is governed by the capacities of the registers Rs and R. The blanking signal BL uses the bit signal Bt4 delayed by half a bit as above stated, and is therefore in synchronism with the clock pulse Cp1.

In a dynamic display system, various conditions may cause non-synchronism between data display signals and display timing signals or overlap of data display signals in the manner as already noted. Either may lead to flickering of the display unit Dp. This flickering can be prevented by the use of the blanking signal BL from the blanking circuit Bc. The flicker-preventing function of the circuit will be explained below with reference to Figure 3.

In Figure 3, waveforms (a) to (e) indicate the time relations among display timing signals Dt_i, Dt_{i+1}, display signals Si, Si+1, and a blanking signal BL in the dynamic display system shown in Figure 1. In this case Dt_i is the i-th display timing signal (1 ≤ i ≤ n) for lighting the display device in the i-th position; Dt_{i+1} is the display timing signal for the next (i+1)-th display device; Si is the display signal in the i-th position to be displayed on the i-th display device by the display timing signal Dt_i; and Si+1 is the display signal for the (i+1)-th position. The display signals Si, Si+1 are, for example, output signals from the decoder circuit Dc. While the blanking signal is at a low level the AND gates A1—Am remain closed, and therefore the display signals S1—Sn are not fed to the drive circuit Dr and the display devices D1—Dn are not lit.

Assuming now that the i-th display signal Si is delayed from the i-th display timing signal Dt_i as indicated in waveforms (a) and (c) in Figure 3, a hatched portion X of the display signal Si for the i-th display device Dpi will tend to be displayed on the display device Dpi+1 in the next position by the action of the following display timing signal Dt_{i+1}, but the blanking signal BL will keep the portion X from being displayed. It will be seen that if the blanking signal BL is not applied the portion X will cause a flicker of the display unit.

Similarly if the (i+1)-th display timing signal Dt_{i+1} lags behind the (i+1)-th display signal Si+1 as shown at waveforms (c) and (d) in Figure 3, a hatched portion Y of the display signal Si+1 to be displayed on the (i+1)-th display device Dpi+1 will tend to be displayed on the display device Dpi in the preceding position. Here again the blanking signal BL will prevent the portion Y from being displayed.

Thus, a blanking pulse Sb is provided which extends over the border time between the i-th display timing signal Dt_i and the following (i+1)-th display timing signal Dt_{i+1} and thereby bridges the two timing

signals, so that neither of the display devices corresponding to the signals is lit during the period equal to the duration of the blanking pulse Sb. Consequently, whether any display signal lags behind a display timing signal or vice versa, the signal portion X or Y that is out of synchronism as shown in Figure 3 is not displayed and, naturally, flickering of the display unit is prevented.

Although the blanking signal BL slightly shortens the lighting time of the display unit (to about three-quarters of the full lighting period), it is practically negligible. Should any problem arise from it, the problem would be readily solved by increasing the voltage applicable to the display unit by the amount proportional to the decrement of the lighting time (while maintaining the power consumption at an unchanged level). It has now been found that where light emitting diodes are employed as the display devices the application of an increased voltage enhances the luminous intensity of the display unit.

Also, in the case where the display signals in the adjacent positions overlap due to the difference between the rise-time characteristics of the active elements that are employed, for example, where as shown in Figure 3(c) and (d), the i -th display signal S_i and the $(i+1)$ -th display signal S_{i+1} overlap in the hatched portions X and Y, it is possible to eliminate the over-lapping portions X and Y by means of blanking signals BL and thereby avoid flickering of the display unit.

The blanking pulses Sb can be formed by staggering one of the bits (e.g., the bit signal Bt4) for use on an electronic desk-top calculator by half a bit by means of a simple arrangement. No complicated circuit is required for this purpose.

In a modified form, the blanking signal BL which is placed in between the drive circuit Dr and decoder circuit Dc in the above-described embodiment, may be placed into or in the front or rear of the decoder circuit Dc or drive circuit Dr, instead, because it has only to shut off the power supply to the display unit. Also the blanking signal BL may be used to control the supply of timing signals to the display unit in place of controlling the supply of display signals to the unit.

Additionally, the display devices need not be Nixie tubes, but may be digitrons (Registered Trade Mark), light emitting diodes, or liquid crystals.

WHAT WE CLAIM IS:—

1. A dynamic display system operating in a time-sharing manner, comprising a plurality of display devices; means for applying consecutive timing signals to the respective display devices for time-sharing energization thereof; means for selectively applying display signals to selected display devices to actuate the display devices in selected combinations, said display devices being energized only upon coincident receipt of a timing signal and a display signal; blanking means for generating blanking signals having a pulse width sufficient to cover the border time between adjacent display or timing signals; and gating means for gating said blanking signals with said display signals or said timing signals so as to prevent application of said display signals or said timing signals during the period of the blanking signals.

2. A dynamic display system according to claim 1, wherein the blanking means includes; a ring counter; a delay means connected to the output of the ring counter; and an inverter connected to the output of the delay means.

3. A dynamic display system according to claim 1 or 2, wherein the gating means includes a plurality of AND gates, each having one input receiving said blanking signal and another input receiving one of said display signals or one of said timing signals.

4. A dynamic display system according to claim 2 or 3, wherein the delay means and the inverter are constituted by insulated-gate field effect transistors.

5. A dynamic display system constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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Although the blanking signal BL slightly shortens the lighting time of the display unit (to about three-quarters of the full lighting period), it is practically negligible. Should any problem arise from it, the problem would be readily solved by increasing the voltage applicable to the display unit by the amount proportional to the decrement of the lighting time (while maintaining the power consumption at an unchanged level). It has now been found that where light emitting diodes are employed as the display devices the application of an increased voltage enhances the luminous intensity of the display unit.
Also, in the case where the display signals in the adjacent positions overlap due to the difference between the rise-time characteristics of the active elements that are employed, for example, where as shown in Figure 3(c) and (d), the i-th display signal Si and the (i+1)-th display signal Si+1 overlap in the hatched portions X and Y, it is possible to eliminate the over-lapping portions X and Y by means of blanking signals BL and thereby avoid flickering of the display unit.
The blanking pulses Sb can be formed by staggering one of the bits (e.g., the bit signal Bt4) for use on an electronic desk-top calculator by half a bit by means of a simple arrangement. No complicated circuit is required for this purpose.
In a modified form, the blanking signal BL which is placed in between the drive circuit Dr and decoder circuit Dc in the above-described embodiment, may be placed into or in the front or rear of the decoder circuit Dc or drive circuit Dr, instead, because it has only to shut off the power supply to the display unit. Also the blanking signal BL may be used to control the supply of timing signals to the display unit in place of controlling the supply of display signals to the unit.

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2. A dynamic display system according to claim 1, wherein the blanking means includes; a ring counter; a delay means connected to the output of the ring counter; and an inverter connected to the output of the delay means.
3. A dynamic display system according to claim 1 or 2, wherein the gating means includes a plurality of AND gates, each having one input receiving said blanking signal and another input receiving one of said display signals or one of said timing signals.
4. A dynamic display system according to claim 2 or 3, wherein the delay means and the inverter are constituted by insulated-gate field effect transistors.
5. A dynamic display system constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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