

Description

Apparatus for the interference-immune modulation and demodulation of analog signals for message transmission via the screens of power transmission cables

5 The invention relates to a circuit which is required at interfaces between the screens of power transmission cables, which screens serve as transmission paths, and the devices for selection and processing of the respective messages, generally digital computers, for
10 feeding in or receiving the messages which are present in the form of analog, frequency-modulated signals. At the transmitting end of the circuit, it is used for the generation of the signals from current digital selection values, that is to say for the so-called modulation. At
15 the receiving end of the circuit, it is used for the recovery of the digital selection values from received analog signals, that is to say for the so-called demodulation. A circuit of this type is also frequently referred to as a modem or a modem circuit.

20 During modulation, sinusoidal, analog signals having two different transmission frequencies, which can be designated as upper frequency and lower frequency, are formed in the transmitting section of a modem. The high-frequency rate of switching over between the transmission
25 frequencies, that is to say the keying which constitutes frequency modulation, depends on the current bit pattern of the respective digital selection value. In this case, one transmission frequency is uniquely assigned to each of the two binary values. During demodulation, that
30 transmission frequency of the two transmission frequencies which is currently being received is identified in the receiving section of a modem. The corresponding binary value is then assigned to this transmission frequency. The digital selection value which represents
35 the respective message is finally reconstructed from the sequence of binary values produced in this way.

 The circuit according to the invention is

employed specifically in so-called cable screen communications. In this case, the messages in the form of analog, frequency-modulated signals are transmitted via the screens particularly of high-voltage cables serving for power distribution. The messages are generally control signals and state indication signals. In this case, control signals are usually generated by a central computer and are used to control network operating equipment in the power distribution network, for example stepping transformers, circuit-breakers and the like. On the other hand, such messages may also be state indication signals, by means of which the current operating state of the power distribution network are communicated to the central computer by the network operating equipment arranged in a distributed manner in the said network.

A problem of cable screen communications is that the power transmission cables are generally constituents of a highly ramified cable network which serves the purpose of supplying power particularly in cities. For this reason, the transmission of the abovementioned control and state indication signals via cable screens is not effected in the form of a simple point-to-point transmission. Rather the analog, frequency-modulated signals must be forwarded with the aid of so-called relay stations via the screens of a chain of interconnected power transmission cables, until they reach the destination relay station. A relay station of this type is usually situated at each node of the power transmission network, that is to say at each point where at least two cable ends meet. This relay station has the task, with the aid of an integrated modem circuit in each case, of receiving analog, frequency-modulated signals from the screen of a power transmission cable and of reconstructing the associated digital selection values. The latter are evaluated in a local digital computer of the modem. Consequently, the modem circuit must be ready to receive in the direction of all the connected cable screens.

The messages may be directed to the relay station

which is doing the receiving at that point. The digital selection values reconstructed therefrom may then turn out to be, for example, control signals relating to the item of network operating equipment situated at the
5 respective network node. On the other hand, they may be, for example, control signals directed from the central computer to an item of network operating equipment situated at a different network node, or, for example, state indication signals directed to the central computer
10 from an item of network operating equipment situated at a specific other network node. In these cases, the analog, frequency-modulated signals must be received by each relay station from the direction of a power transmission cable and be demodulated. Only then is it
15 possible to identify their addressing, directed to a different relay station or to the central computer, in the local digital computer of the respective modem. They are then modulated anew and fed in the direction of the corresponding power transmission cable, into the cable
20 screen thereof. It is also possible for an item of network operating equipment independently to generate a state indication which then feeds via the modem of the local relay station, usually in the direction of the central computer, into the cable screen of the corresponding
25 power transmission cable.

The cable screen network used for transmission consequently has a very special topology. This is characterized, in particular, by the interfaces of the cable screens at the nodes of the power transmission
30 network, which interfaces are occupied by relay stations and an integrated modem circuit in each case. These nodes constitute points of interruption in the transmission path comprising the chain of cable screens. For this reason, particularly high requirements must be made of
35 the quality of the message transmission. Consequently, the modulation and demodulation in the modem of each relay station must be particularly robust, that is to say insensitive to the coupling-in of interference which may occur during the transmission into any cable screen or at

one of the many nodes.

The invention is based on the object of specifying a modem circuit which is as simple as possible yet which permits messages to be coupled into and out of the screens of power transmission cables with high interference immunity.

The object is achieved by means of the circuit specified in Claim 1. Advantageous further embodiments are specified in the subclaims.

The invention and advantageous further embodiments of the invention are explained in more detail with reference to the figures which are briefly referred to below and in which:

Figure 1 shows a block diagram of the modem circuit according to the invention for feeding messages into, and coupling them out of, the screens of power transmission cables,

Figure 2 shows an advantageous design of a clocked bandpass filter in the modem circuit according to the invention,

Figure 3 shows the signal characteristic of an advantageous embodiment of a Schmitt trigger in the receiving section of the modem circuit according to the invention,

Figure 4 shows the signal characteristic at the input of an advantageous embodiment of a digital demodulator in the receiving section of the modem circuit according to the invention,

Figure 5 shows the signal characteristic of an advantageous embodiment of a digital modulator in the transmitting section of the modem circuit according to the invention,

Figure 6 shows the signal characteristic of an advantageous embodiment of a low-pass filter at the output of the transmitting section of the modem circuit according to the invention, and

Figure 7 shows the example of a two-channel design of the modem circuit according to the invention.

Figure 1 shows the block diagram of the modem

circuit according to the invention. For better clarity, a vertical separating line A-D and a horizontal separating line E-S are drawn in this diagram. The horizontal separating line E-S demarcates the receiving section E and the transmitting section S of the modem circuit. A
5 respective analog section A and a respective digital section D, that is to say a respective section in which analog signal processing or digital signal processing, respectively, is carried out, are additionally demarcated
10 in the receiving and transmitting sections E, S of the modem circuit by the vertical separating line A-D.

 The analog, frequency-shift-keyed signals fed into the power transmission network by another modem are drawn from the receiving section E of the circuit according to the invention as reception signals EK from the
15 screen of the respectively adjacent local power transmission cable and fed in on the left-hand side in Figure 1. These signals are conditioned in the analog section of the receiving section E, in a bandpass filter GT which is
20 clocked by means of a central precision clock signal T, and are fed to a Schmitt trigger ST which forms the interface between the analog and digital sections of the receiving section E. From the conditioned analog reception signals, the said Schmitt trigger derives
25 rectangular-waveform trigger signals TR, which are fed as control signals to a digital demodulator DDM, which is likewise operated by the central precision clock signal T. The said demodulator demodulates the trigger signals TR by determining the current transmission frequency of
30 the reception signals, that is say by detecting the upper or lower frequency, and assigns the respective binary value to them. The stream of demodulated bits produced in this way is fed in the form of a serial reception bit stream EBS to the data input of a local computer CPU. The
35 latter finally decodes the actual selection values, that is to say the respective message content, from the current "pattern" of the bit stream EBS.

 If a modem of the type illustrated in Figure 1 is contained in a so-called head end, the computer CPU gen-

erally communicates via an output data bus ADB with a central computer KP. The latter organizes the message transmission and thus the control of an entire power transmission cable network. On the other hand, a modem
5 according to the circuit of Figure 1 is contained in each of the relay stations distributed in a power transmission cable network. In this case, the computer CPU communicates via the output data bus ADB with the control elements of the respective item of network operating
10 equipment.

In the transmitting section S of the inventive circuit of Figure 1, updated digital selection values are fed, in the form of a preferably pulse-interval-modulated serial transmission bit stream SBS, from the local
15 computer CPU of the modem to a digital modulator DM, which is likewise operated by the central precision clock signal T. At the output of the digital modulator DM, rectangular signals having the upper or lower frequency are generated as a function of the current value of the
20 transmission bit stream SBS. The signals are finally converted into sinusoidal transmission signals in a low-pass filter TP, which constitutes the interface between the digital and analog sections of the transmitting section S of the circuit according to the invention, and
25 then fed into the screen of power transmission cables.

The centrepiece, of the modem circuit according to the invention is the control of the essential elements of the circuit both on the receiving side E and on the transmitting side S by means of a central precision
30 control clock signal T as a common time base or reference. This clock signal is fed as a common time base at least to the clocked bandpass filter GT, to the digital demodulator DDM and to the digital modulator DM. From this time base, all of these elements can derive different
35 frequencies that are respectively required with high accuracy. On account of this close tuning of the essential elements to one another, and in particular of the operations that they carry out, namely modulation at the transmitting end and demodulation at the receiving end,

particularly precise modulation and demodulation of transmitted signals is possible, that is to say narrow-band and thus interference-immune transmission overall. The central precision control clock signal T can be
5 provided by a separate precision clock generator PT, as is illustrated in the example of Figure 1. On the other hand, it is also possible for the precision clock signal to be generated with high accuracy in the computer CPU.

The inventive central generation of a precision
10 control clock signal T for all the essential elements of the modem circuit of Figure 1 has a large number of advantages. On the one hand, the circuitry for signal conditioning is considerably reduced on the analog side A of the receiving section E by the enabling of the use
15 of a clocked bandpass filter GT for conditioning the reception signals EK, and on the digital side A of the receiving section E by the enabling of the use of a digital demodulator DDM. In the same way, the circuitry is considerably reduced at the transmitting end S by the
20 enabling of the use of a digital modulator DM.

Nevertheless, the circuit design according to the invention achieves a considerable improvement in the insusceptibility to interference during signal processing both with regard to the demodulation of received signals
25 and during the modulation of signals to be transmitted. The improvement in quality of the modulation of signals to be transmitted in turn benefits the signal processing at the receiving end of another modem circuit, arranged in a relay station at a different point in the power
30 distribution network, during the reception and demodulation taking place in the said circuit. This can be attributed to the rigid locking of the receiving end E and of the transmitting end S by means of the central precision control clock signal T. The more accurately the
35 transmission bit stream SBS is converted at the transmitting end S into analog, sinusoidal transmission signals with reference to the central precision control clock signal T, the more easily and more accurately an equivalent reception bit stream EBS can be received,

conditioned and reconstructed in a corresponding modem at a different point in the power transmission network. The inventive configuration of the modem circuit consequently benefits the transmission quality of the entire message transmission via the cable screens of the power transmission cables. In particular, this causes the circuit to be less susceptible to the coupling-in of interference which can occur to a particularly large extent precisely in the event of message transmission via the screens of power transmission cables.

Furthermore, the circuit design according to the invention makes it possible to achieve particularly narrowband transmission. Consequently, the circuit design according to the invention is particularly suitable for the use of two characteristic frequencies whose values are close together. The upper and lower frequencies may consequently be separated merely by an unusually small carrier frequency shift of about 0.5 kilohertz, for example. Specifically, particularly high frequency stability can be achieved by the quasi-synchronous control of the clocked bandpass filter GT, of the digital demodulator DDM and of the digital modulator DM by means of the central precision clock signal T. It is consequently possible to modulate in a simple manner at the transmitting end even upper and lower frequencies which are close together, and, in particular at the receiving end, to demodulate them again simply and in a manner immune to interference. Consequently, the suppression of interference which is coupled into the analog, frequency-modulated signals on the screens of the power transmission cables is particularly effective.

The clocked bandpass filter GT in the analog Section A of the receiving Section E of the circuit according to the invention has the task at least of conditioning the analog reception signals EK in such a way that the interfering high frequency components and interfering low frequency components, which are similar to a DC voltage offset, are filtered out. Consequently, the frequency spectrum of the filtered analog signals is

clipped in such a way that the only frequencies contained are those from a band lying as close as possible around the between the upper and lower frequency values used for the modulation. According to the invention, the mid-frequency of the clocked bandpass filter GT is derived from the central precision clock generator PT of the circuit. Since the mid-frequency can be predetermined in a very accurate and stable manner by this means, the transmission can advantageously be designed with a narrowband nature. The filter mid-frequency then lies as accurately as possible in the middle of the upper and lower frequencies between which keying is effected during the modulation and demodulation. This considerably improves the interference immunity of the data transmission.

The analog reception signals EK conditioned by the clocked bandpass filter GT are then fed to a Schmitt trigger ST. The latter forms the interface between the analog section A and the digital section D of the circuit according to the invention. The Schmitt trigger ST contains at least one comparator, by means of which the conditioned reception signals EK are converted into at least one rectangular signal TR at the same frequency. This is used in turn to trigger the following digital demodulator DDM.

The digital demodulator DDM has the task of detecting the frequency of the analog reception signals EK and of unambiguously assigning to this frequency as far as possible the upper or lower frequency value. For this purpose, the digital demodulator has at least one reference counter, to which the trigger signal TR from the Schmitt trigger ST is fed. The said counter counts out the period of each oscillation, that is to say the the interval between the trigger signals TR, thereby producing a measured frequency value. According to the invention, the counting clock signal of the reference counter is likewise determined by the central precision clock signal T of the precision clock generator PT. In this case, too, the precision clock signal T again

fulfils the function of a central time base for the entire modem circuit. As a result, the frequency markers necessary for the frequency identification can be set precisely. Consequently, the swing of the carrier frequency can be small, so that the resultant narrowband nature of the transmission brings about a considerable improvement in the insusceptibility of the modem circuit according to the invention to interference. Furthermore, on account of the digital design of the demodulator DDM, tolerances, temperature drifting and ageing-induced level shifts do not occur. The outlay on hardware is greatly reduced by this design without any losses in the demodulation accuracy. The digital demodulator can be produced using simple digital modules such as, for example, gates, flip-flops, counters. In contrast to this, the outlay on hardware is considerably greater in known demodulator circuits, for example in the case of an intermediate frequency demodulator, a quadrature decoder or a phase locked loop demodulator.

The circuit according to the invention is optimally matched to the specific boundary conditions existing for data transmission via the screens of high-voltage cables. Despite a reduced outlay on hardware, the modem circuit portrayed above achieves particularly high interference immunity for data transmission using a narrowband transmission spectrum.

Preferred further embodiments of the invention are explained, inter alia, with reference to the following Figures 2 to 7.

The clocked bandpass filter GT is advantageously realized in the form of a clocked capacitor filter. Filters of this type are also referred to as "switched capacitor filters". In the case of this clocked filter, it is possible to dispense with an external circuit having real capacitors for the determination of the frequency properties. The said real capacitors would have to be very accurate and have a good temperature and ageing behaviour, and would consequently be expensive. The position of the pole points of the filter is instead

determined by the value of the central precision clock signal T and a simple, external resistor circuit. Despite the simple structure of such a filter, the latter has a very high quality and reproducible filter properties. It is advantageous if the clocked bandpass filter GT comprises a cascade of a plurality of subfilters. It can be constructed, for example, as a block of four universal switched-capacitor subfilters. In this case, the four subfilters are advantageously cascaded and the pole points of the subfilters are placed one on the other. As a result, it is possible overall to achieve good frequency selectivity despite the limited qualities of the subfilters. Given a carrier frequency shift of about 0.5 kilohertz, for example, the bandwidth of the clocked bandpass filter is preferably about 1.8 kHz.

The clocked bandpass filter GT can advantageously be supplemented by an additional prefilter and, if appropriate, an additional postfilter. A filter chain GT of this type is illustrated in the example of Figure 2 and comprises a prefilter VF, the actual clocked bandpass filter BF and a postfilter NF.

The analog reception signals EK drawn from the screen of a power transmission cable are advantageously subjected to a first processing in a prefilter VF having the properties of a bandpass filter. By utilizing the low-pass filter properties of the prefilter, particularly high, interfering frequency components can be filtered out to prevent them from being looped in right at the input of the modem circuit according to the invention. This improves the susceptibility of the circuit to interference. Furthermore, the configuration and dimensioning of the further elements in the receiving section of the circuit, in particular of the clocked bandpass filter BF and of the digital demodulator DDM, are considerably simplified. By utilizing the high-pass filter properties of the prefilter, it is possible to suppress a so-called DC component, also called offset, in the lower frequency range. This also considerably simplifies the configuration and dimensioning of the further circuit

sections and, in particular, improves their method of operation, since by avoiding a possible DC component, it is possible to maintain the input dynamic range at the following filters.

5 The prefilter VF is advantageously designed in the form of an active, continuous bandpass filter, preferably a 1st-order one, and realized using an operational amplifier and RC circuit, for example. This filter can advantageously be used, inter alia, as a so-called anti-aliasing filter for the following, clocked bandpass filter BF. Since the actual "filtering task" is carried out by the following, clocked bandpass filter BF, the filter mid-frequency of which is tuned by means of the central precision clock signal T exactly to the
10 respective values of the upper and lower frequency, the bandwidth and the cut-off frequencies of the prefilter VF do not have to be tuned exactly to the frequency conditions present during modulation and demodulation. Complicated circuit measures for keeping them constant can thus
15 advantageously be avoided. Only approximate tuning is also sufficient for the suppression of a DC component.

 Advantageously, the prefilter VF additionally contains means for setting the gain. This enables the signal level of the received, analog input signals EK to
25 be matched to the input voltage range of the downstream elements of the circuit, in particular of the bandpass filter. On the one hand, this advantageously ensures a minimum value of the signal level which is required for the further signal processing. On the other hand, this
30 avoids the situation where the exceeding of a maximum signal level causes the elements which follow in the receiving section of the modem circuit according to the invention to be overdriven. The setting of the gain as early as in the prefilter VF has the particular advantage
35 that it is not necessary to carry out any more amplification in the rest of the circuit. The amplification of the analog reception signals EK as early as in the prefilter VF has the advantage that a gain in the noise generated by the further elements in the receiving section E of the

circuit, in particular the noise of the clocked bandpass filter BF, the maximum of which lies precisely in its own passband, is not concomitantly amplified. The signal-to-noise ratio can be considerably improved by this means.

5 Advantageously, the analog input signals can be conditioned further by an additional postfilter NF downstream of the clocked bandpass filter BF. On the one hand, this makes it possible to attenuate any noise which possibly occurs at the output of the clocked bandpass
10 filter BF, particularly when the latter is designed as a switched capacitor filter, and which is also referred to as clock feedthrough or crosstalk of the bandpass clock. On the other hand, this makes it possible to suppress a DC component which is possibly produced in the clocked
15 bandpass filter BF, with the result that the reception signal remains balanced with respect to the reference earth of the circuit. Noise-free and balanced reception signals actively support the error-free conversion thereof into rectangular signals in the downstream
20 Schmitt trigger ST. The postfilter NF can advantageously be realized as an active, continuous bandpass filter, preferably a 1st-order filter, using an operation amplifier and RC circuit, for example. On account of the advantageous structure of the modem circuit according to
25 the invention, as in the case of the prefilter VF, it is also unnecessary in the case of the postfilter NF to impose high requirements on maintaining exact values of bandwidth and cut-off frequencies.

30 The clocked bandpass filter GT, which, in accordance with the illustration in Figure 2, preferably comprises a chain formed by the prefilter VF, the clocked bandpass filter BF and the postfilter NF, conditions the analog reception signals EK in such a way that interfering high-frequency components and low-frequency offset
35 components similar to DC voltage are filtered out, and that the signals have a sinusoidal waveform which is balanced with respect to the analog reference earth of the circuit.

 The signal characteristic of a preferred exemp-

lary embodiment for a Schmitt trigger ST is illustrated in Figure 3. The said Schmitt trigger forms the interface between the analog and digital receiving section E. A sinusoidal reception signal EK which has been filtered by means of the clocked bandpass filter GT and is balanced with respect to the analog earth of the modem circuit is converted in the Schmitt trigger ST, preferably by means of two comparators, into two complementary rectangular signals /S and /R with the same frequency. These signals are a digitized representation of the analog reception signal EK. In this embodiment, the rectangular signals /S and /R represent the output signal "TR" of the Schmitt trigger ST.

Advantageously, the Schmitt trigger additionally has means which make it possible to predetermine for the comparators a respective threshold voltage value $+U_h$ and $-U_h$ lying above and below, respectively, the reference earth of the modem circuit. The effect of this is that the comparators do not switch at the zero crossing of the sinusoidal reception signal EK, but rather only on each occasion when a threshold voltage $+U_h$ or $-U_h$ is reached. The resultant switching hysteresis causes the Schmitt trigger to switch independently of the so-called fundamental noise and in a manner free from jitter. This advantageously effects noise suppression. The magnitude of the threshold voltage U_h is preferably adjustable. As a result, the sensitivity of the Schmitt trigger ST can be tuned to the current noise conditions on the cable screens serving as a transmission path. Furthermore, precise setting of the two threshold voltages is, however, unnecessary with regard to the frequency identification. Since the comparators in the Schmitt trigger switch at the same point in each period, the magnitude of the threshold voltage does not affect the frequency of the rectangular signals /S, /R. The frequency of the latter is maintained and hence so is their function as trigger signals with the same frequency for the digital demodulator DDM.

The signal characteristic at the input of a

preferred embodiment of the digital demodulator DDM is illustrated in the example of Figure 4.

According to this design, the digital demodulator DDM preferably has at its input an RS flip-flop, to whose
5 level-sensitive set and reset inputs the trigger signals /S and /R of the Schmitt trigger ST are fed. The complementary flip-flop outputs Q and /Q are set thereby. A flip-flop with level-active set and reset inputs advantageously suppresses any oscillation which might still be
10 present in the /S and /R signals, designated by bouncing in Figure 4. The positive edges of the /Q signal are differentiated in the digital demodulator DDM and an internal trigger signal TS is generated from this. The frequency of the said internal trigger signal corresponds
15 to the frequency of an analog reception signal EK.

A sequence controller in the digital demodulator DDM is triggered by each positive edge of the internal TS trigger signal. The time between the positive trigger edges can be measured by a reference counter driven by
20 the central precision clock signal T, and the counter reading can be evaluated by a digital window comparator.

In this case, the counter reading of the reference counter is preferably compared with three comparison values, which correspond to three frequency markers. This
25 forms, as it were, a double frequency window. One of the three frequency markers serves as the so-called mid-frequency between the upper and lower frequencies. As a result, in the demodulator it is possible to identify whether a received instantaneous frequency is greater or
30 less than the mid-frequency, and, consequently, whether it is to be assigned either to the upper frequency or to the lower frequency. In order to limit this double frequency window, use is made of an additional upper frequency limit and of an additional lower frequency
35 limit. In the demodulator it is then also possible to identify whether an impermissible frequency lying outside the permissible range of values has been received, that is to say whether the current instantaneous frequency is greater than the upper frequency limit or less than the

lower frequency limit. If one of the two cases is present, then a frequency error signal is generated. By this means, it is possible to signal the presence of a transmission which is subjected to interference. Consequently, this represents a further means for increasing the security of the transmission. The cut-off frequencies of a window comparator can likewise be set by means of the central precision clock signal T.

In the transmitting section S of the inventive circuit of Figure 1, the digital selection values output at the data output of the computer CPU are converted by a digital modulator DM into analog sinusoidal oscillations whose frequency is shifted between the upper and lower frequencies in accordance with the serial transmission bit stream SBS. For this purpose, the modulator advantageously contains a digital frequency generator, which is switched over between the two characteristic frequencies. On account of the circuit design according to the invention, the digital frequency generator is very accurate in terms of frequency, since the respective values of the upper and lower frequencies in the modulator are, according to the invention, derived from the central precision clock signal T. The digital frequency generator switches over between the two characteristic frequencies approximately without any delay.

The signal characteristic of an advantageous embodiment of a digital modulator DM in the transmitting section S of the modem circuit according to the invention is illustrated by way of example in Figure 5.

The so-called continuous phase frequency shift keying modulation method is preferably employed in the digital modulator DM. In this case, there is a switch-over between the upper frequency FL and the lower frequency FH. After the digital modulator DM has been activated by means of a control signal SP, the upper or lower frequency is generated in accordance with the respective logic level of the transmission bit stream SBS which is fed serially to the digital modulator DM by the computer CPU. In the example of Figure 5, the current bit

of the transmission bit stream SBS has a high level after enabling the modulator. During this time, by way of example, an analog signal having the lower frequency FL is transmitted. In the second half of the enabled period of the modulator, the current bit of the transmission bit stream SBS has a low level. During this time, an analog signal which has the upper frequency FH is then transmitted. In Figure 5, the keying between the upper and lower frequencies FL and FH is also marked by a falling edge in the profile of the transmission bit stream SBS.

The frequency shift keying is advantageously carried out when a zero crossing occurs in the respectively active upper-frequency or lower-frequency transmission signal. This is effected by employing a so-called phase-coherent continuous phase frequency shift keying modulation in the digital modulator DM. This is illustrated in Figure 5 by the sampling with the signal MOD. The resultant suppression of the sudden phase changes admittedly causes a slight keying delay, which is likewise shown in Figure 5. A simple logic arrangement is sufficient to suppress the sudden phase changes.

The digital design of the modulator has the advantage that a changeover between two separate, non-synchronizable oscillators with differing frequencies is unnecessary. Such a design would have a large number of disadvantages. Thus, greater sudden phase changes would inevitably occur during the frequency shifting. In order to compensate for them, the bandwidth to be transmitted would have to be increased, which would in turn have an adverse effect on the insusceptibility to interference. Since use is not made of two analog oscillators for the generation of the two characteristic frequencies, settling times which may lie in the milliseconds range do not occur either. Such settling times would be required by each of two separate oscillators, since the latter, when changed over, would have to settle anew between each time. Instead, the inventive design is based on a digital modulator which has a single digital frequency generator driven by the central precision clock signal T. The said

generator can be switched over between the upper and lower frequencies virtually without any delay.

It is advantageous if a low-pass filter TP additionally follows the digital modulator DM at the transmitting end S. By this means, the occurrence of high frequencies which have an interfering effect particularly on the further signal processing can be limited from the outset. Preferably, the low-pass filter TP additionally contains a trapezium generator. By this means, the transmission signal is converted into a symmetrical trapezoidal signal waveform. Figure 6 illustrates the transmission signal of an advantageous embodiment of such a low-pass filter TP at the output of the transmitting section S of the modem circuit according to the invention. The low-pass filter at the same time constitutes the interface between the digital section D and the analog section A. This has the advantage that the further processing of the now quasi-analog transmission signal, in particular the filtering thereof at the receiving end of another modem circuit, is made considerably easier. Harmonics which may possibly have an interfering effect consequently do not even occur in the first place. Thus, on account of the trapezoidal waveform, the 3rd harmonic is omitted, and the 5th harmonic is already considerably attenuated. This trapezium generator in the low-pass filter can be realized using just one operational amplifier. A subsequent simple 2nd-order low-pass filter suffices to suppress the harmonics in the upper range once again. This 2nd-order low-pass filter can likewise be realized using an operational amplifier with RC circuit. With this circuit design, it is possible, using just two operational amplifiers, to generate from a rectangular signal a frequency-modulated sinusoidal signal which has a low harmonics content and is thus easy to transmit and demodulate.

Finally, Figure 7 shows a two-channel design of the modem circuit according to the invention. The channel 1 at the receiving end E in this case comprises a clocked bandpass filter GT1, a Schmitt trigger ST1 and a digital

demodulator DDM1. The clocked bandpass filter GT1 again advantageously comprises a chain containing a prefilter VF1, a clocked bandpass filter BF1 and a postfilter NF1. The channel 2 at the receiving end E in this case comprises, in the same way, a clocked bandpass filter GT2, a Schmitt trigger ST2 and a digital demodulator DDM2. The clocked bandpass filter GT2 again advantageously comprises a chain containing a prefilter VF2, a clocked bandpass filter BF2 and a postfilter NF2. Such a [lacuna] of analog reception signals simultaneously from two transmission directions is possible. This case occurs particularly at the connection points of the screens of two power supply cables.



Patent claims

1. Apparatus for the interference-immune modulation and demodulation of analog signals which are transmitted in a frequency-modulated manner via the screens of power transmission cables, in which
 - a) at least a series circuit formed by a clocked band-pass filter (GT), a Schmitt trigger (ST) and a digital demodulator (DDM) is present at a receiving end (E), and at least a digital modulator (DM) is present at a transmitting end (E), and
 - b) means (PT; CPU) for generating a central precision clock signal (T) are present, which precision clock signal is fed as a common time base at least to the clocked bandpass filter (GT) and to the digital demodulator (DDM) at the receiving end (E) and to the digital modulator (DM) at the transmitting end (S).
2. Apparatus according to Claim 1, in which the digital modulator (DM) at the transmitting end (S) contains at least one digital frequency generator which is driven by the central precision clock signal (T) and derives the characteristic frequencies (FL, FH) for the frequency modulation of selection values to be transmitted from the precision clock signal (T) with high accuracy.
3. Apparatus according to Claim 2, in which digital selection values to be transmitted are subjected to FSK modulation (frequency shift keying modulation) in the digital modulator (DM) by means of modulation-controlled keying of the digital frequency generator between an upper and a lower frequency as characteristic frequencies.
4. Apparatus according to Claim 2 or 3, in which the digital frequency generator in the digital modulator (DM) switches over between the upper and lower frequencies in a phase-coherent manner only upon the occurrence of a zero crossing in one of the characteristic frequencies.
5. Apparatus according to one of the preceding



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claims, in which a low-pass filter (TP) is connected downstream of the digital modulator (DM) at the transmitting end (S).

5 6. Apparatus according to Claim 5, in which the low-pass filter (TP) contains a trapezium generator.

7. Apparatus according to one of the preceding claims, in which the clocked bandpass filter (GT) is designed as a clocked capacitor filter (switched-capacitor filter) and the mid-frequency of the bandpass
10 filter (GT) is determined by the central precision clock signal (T).

8. Apparatus according to one of the preceding claims, in which a prefilter (VF) which is designed as an active continuous bandpass filter, preferably a 1st-order
15 one, is connected upstream of the clocked bandpass filter (GT).

9. Apparatus according to Claim 8, in which the prefilter (VF) has means for setting the gain of the signal levels.

20 10. Apparatus according to one of the preceding claims, in which a postfilter (VF) which is designed as an active continuous bandpass filter, preferably a 1st-order one, is connected downstream of the clocked bandpass filter (GT).

25 11. Apparatus according to one of the preceding claims, in which the digital demodulator (DDM) contains a reference counter for counting out the periods of analog reception signals (EK), the counting clock signal of which counter is determined by the central precision
30 clock signal (T).

12. Apparatus according to Claim 11, in which a flip-flop having level-sensitive set and reset inputs is present at the input of the digital demodulator (DDM).

35 13. Apparatus according to one of the preceding claims, in which the Schmitt trigger (ST) has means for predetermining a threshold voltage ($\pm U_h$), for producing a switching hysteresis.