

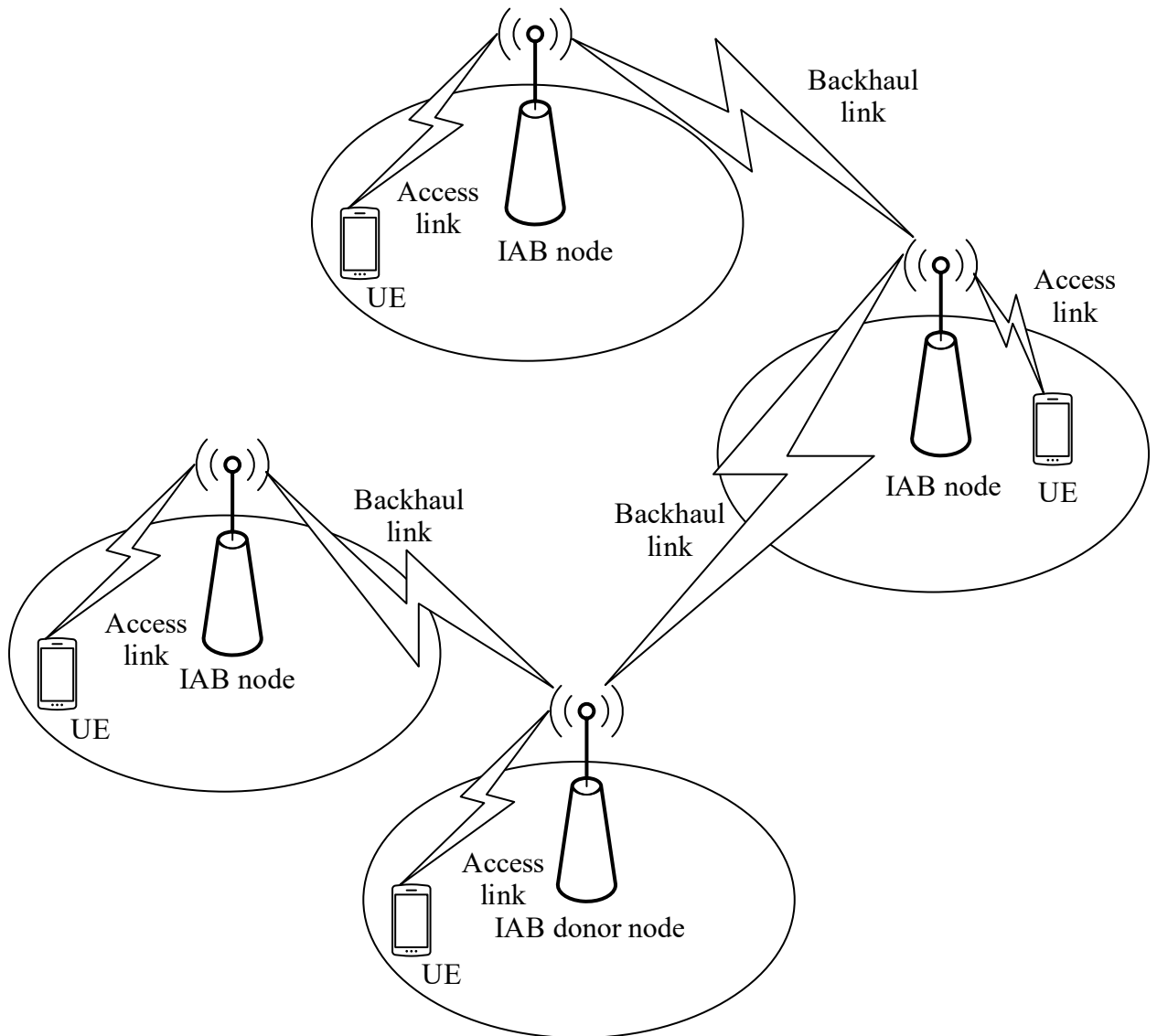


FIG. 1

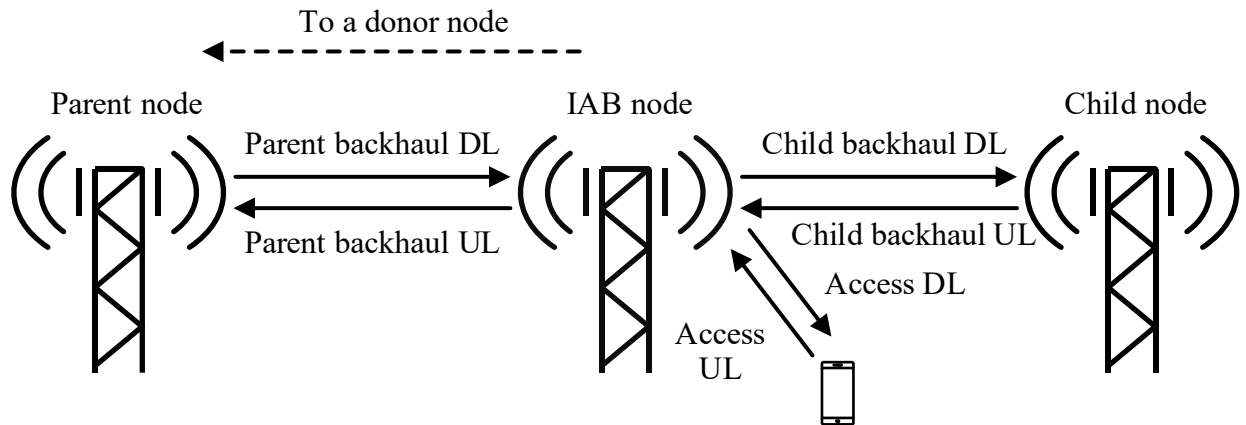


FIG. 2

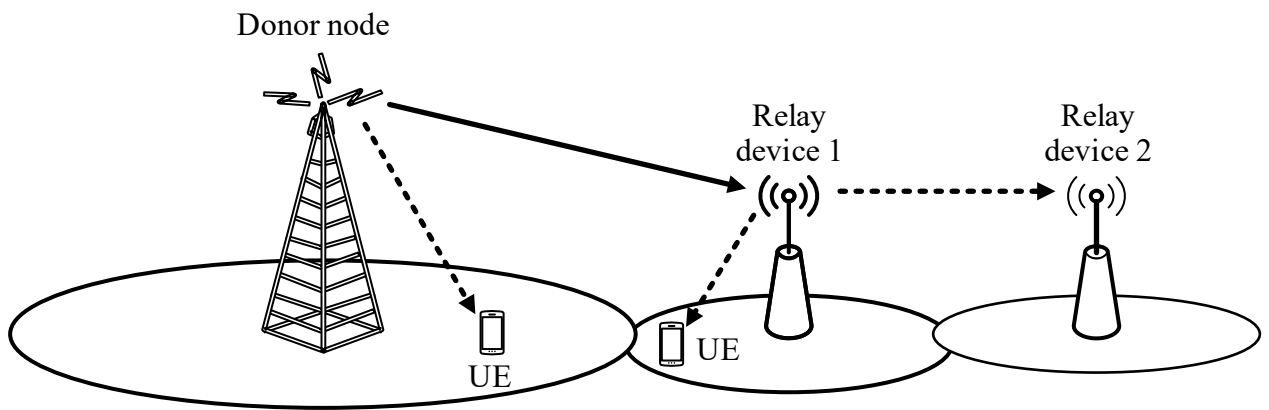


FIG. 3

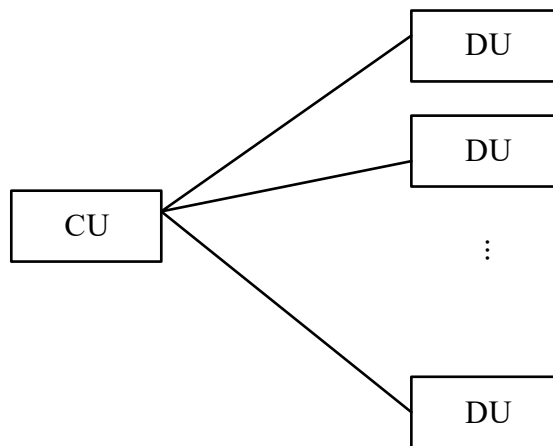


FIG. 4

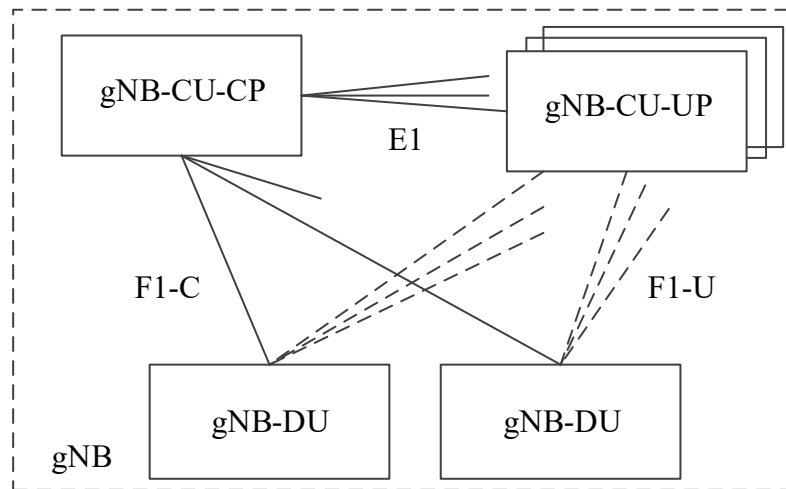


FIG. 5

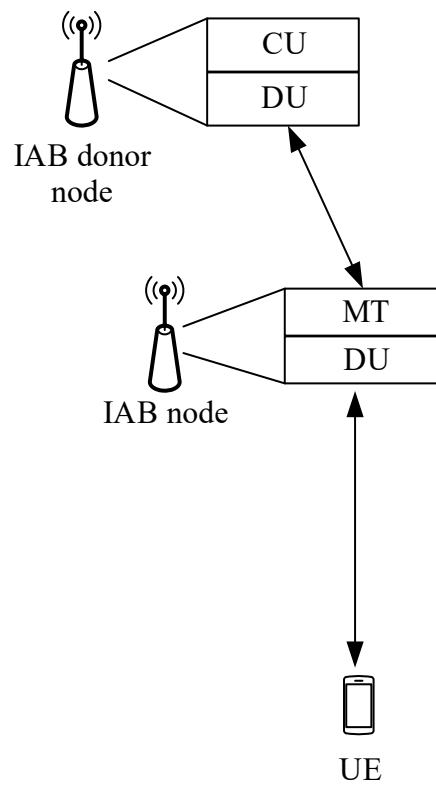


FIG. 6

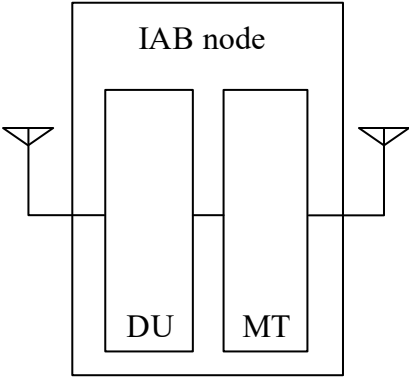


FIG. 7

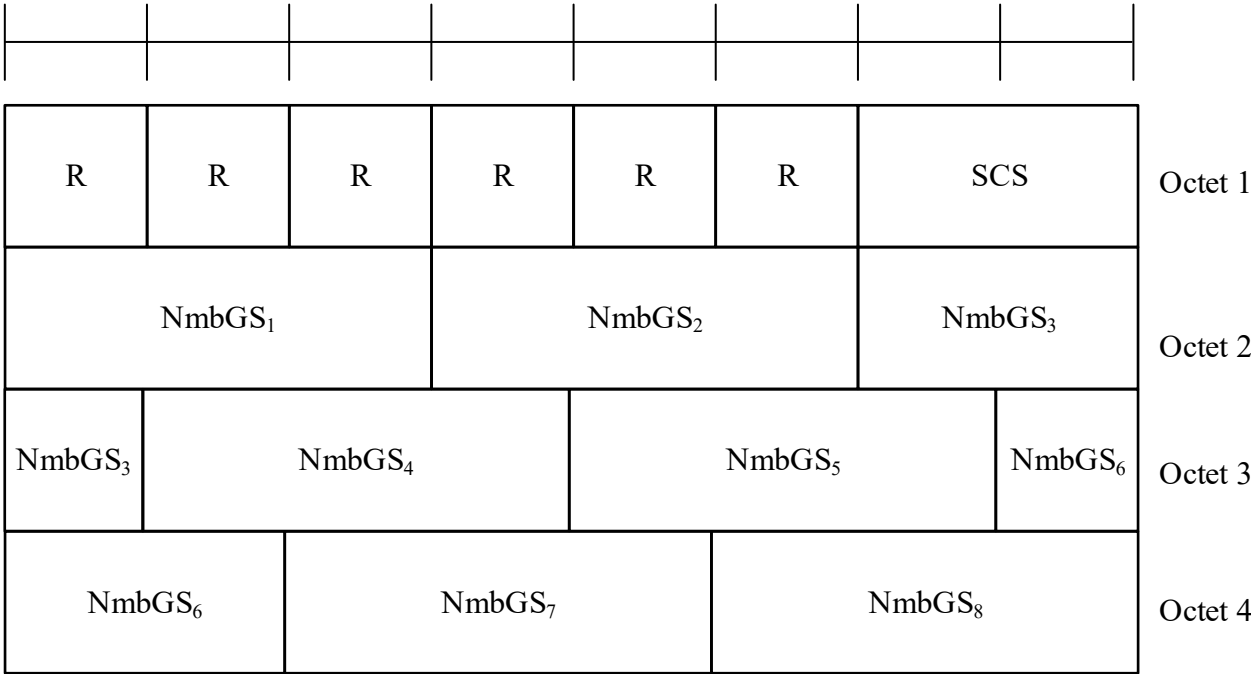


FIG. 8

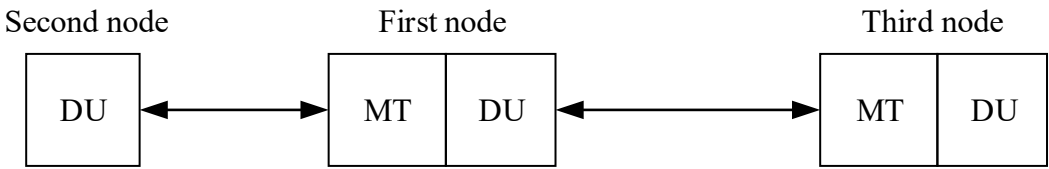


FIG. 9

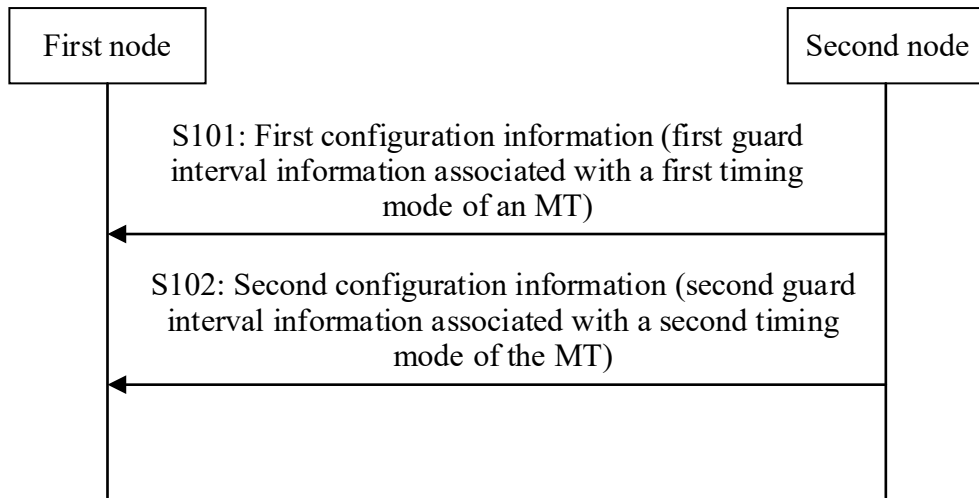


FIG. 10

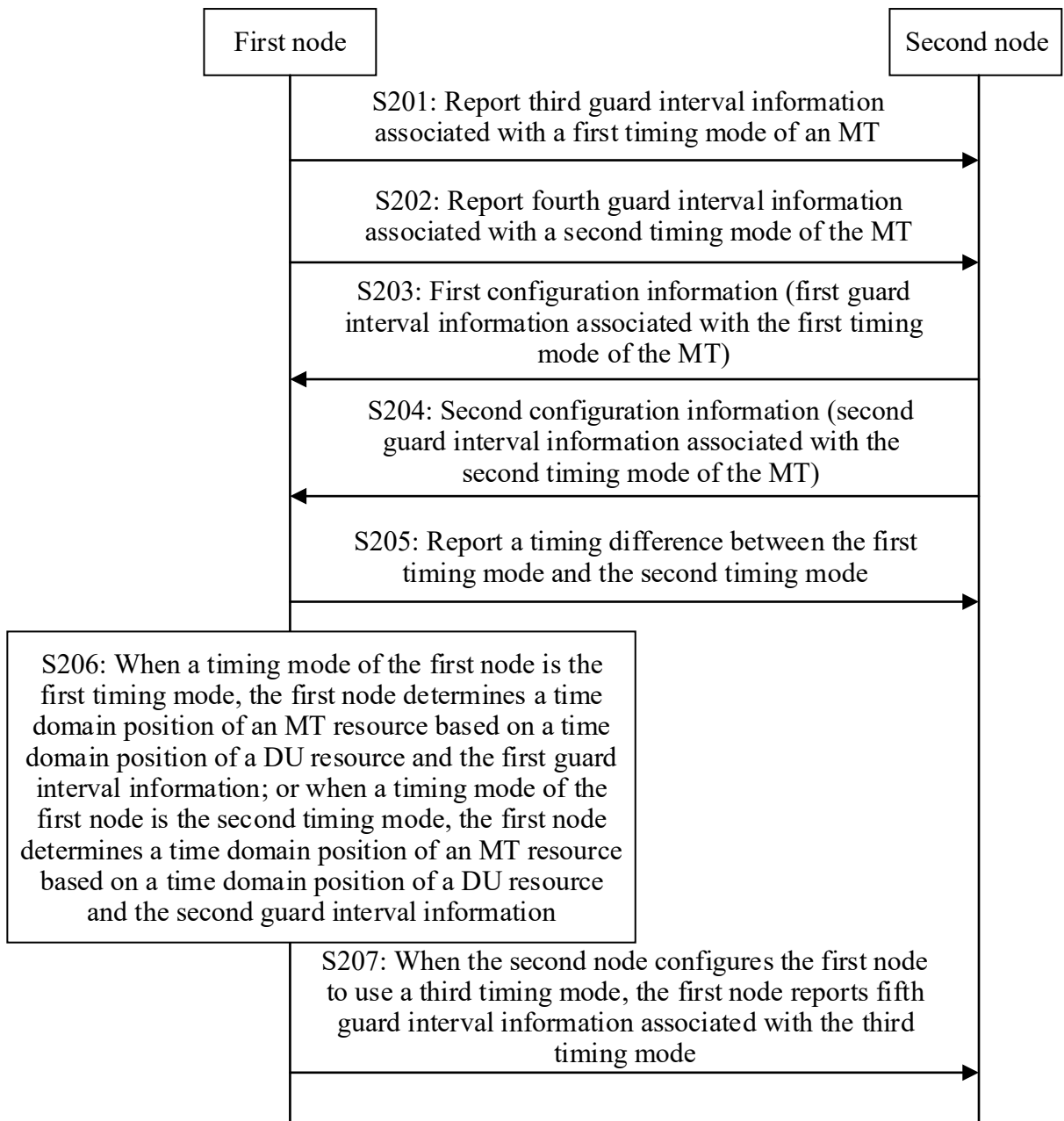


FIG. 11

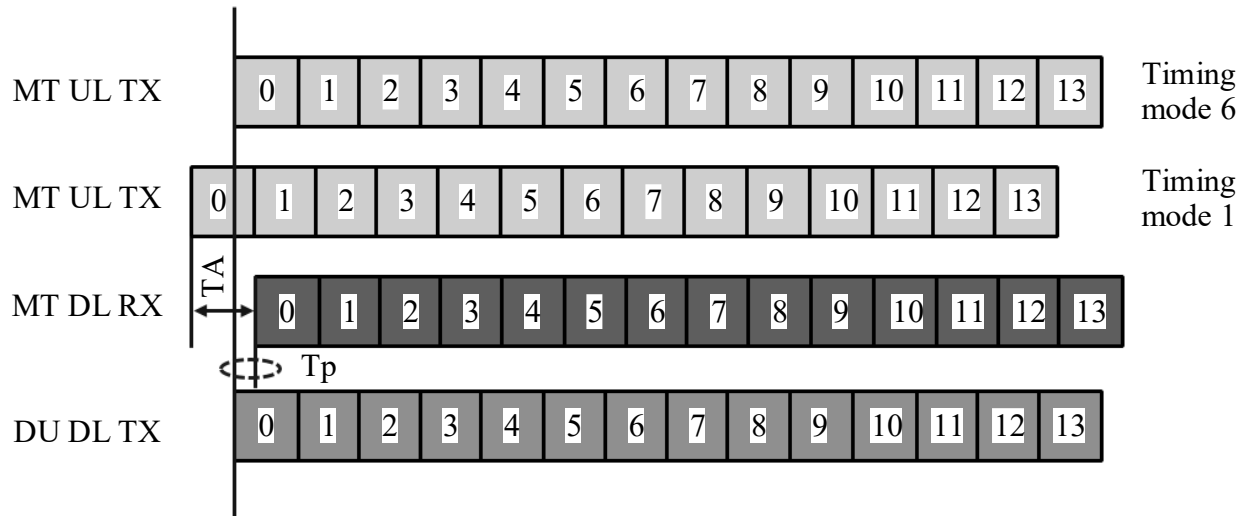


FIG. 12

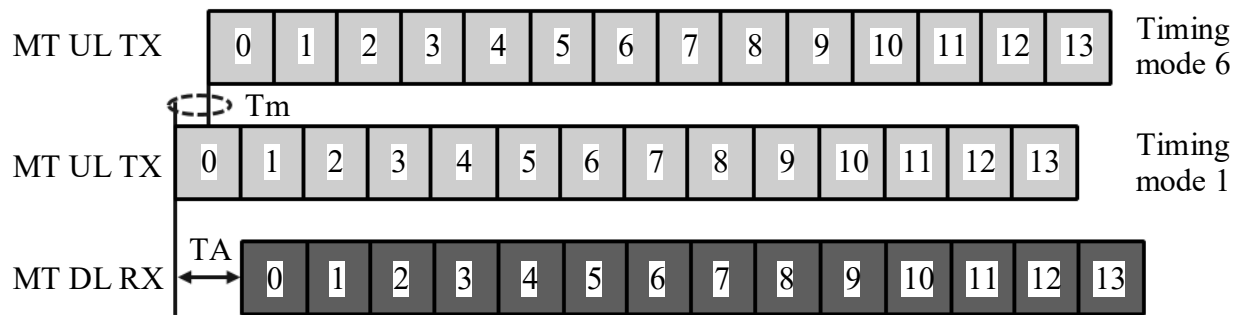


FIG. 13

R	R	R	R	Timing mode	SCS	Octet 1	
NmbGS ₁			NmbGS ₂		NmbGS ₃	Octet 2	
NmbGS ₃	NmbGS ₄			NmbGS ₅		NmbGS ₆	Octet 3
NmbGS ₆		NmbGS ₇			NmbGS ₈		Octet 4

FIG. 14a

R	R	R	Timing mode	R	SCS	Octet 1	
NmbGS ₁			NmbGS ₂		NmbGS ₃	Octet 2	
NmbGS ₃	NmbGS ₄			NmbGS ₅		NmbGS ₆	Octet 3
NmbGS ₆		NmbGS ₇			NmbGS ₈		Octet 4

FIG. 14b

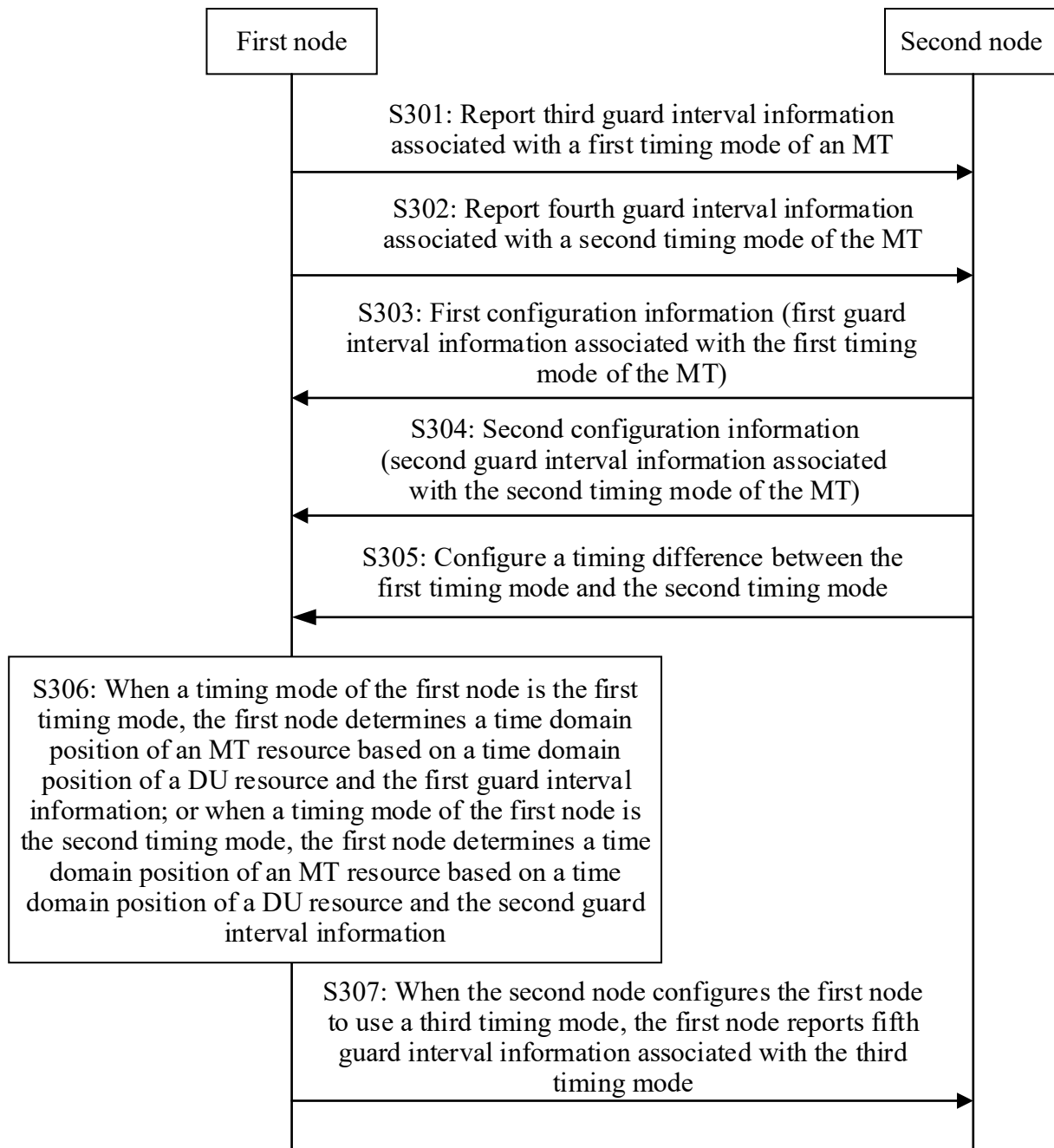


FIG. 15

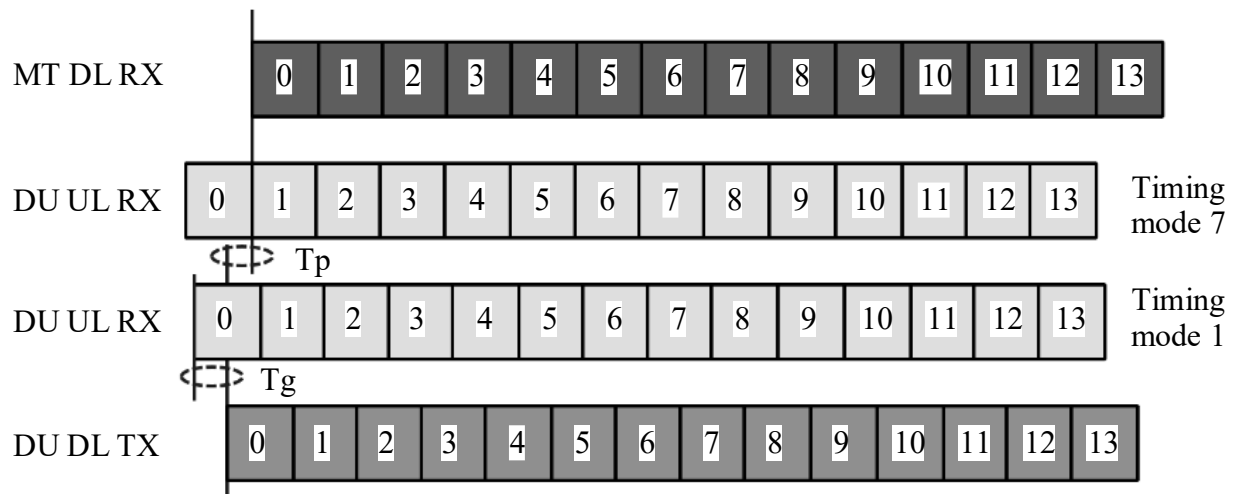


FIG. 16

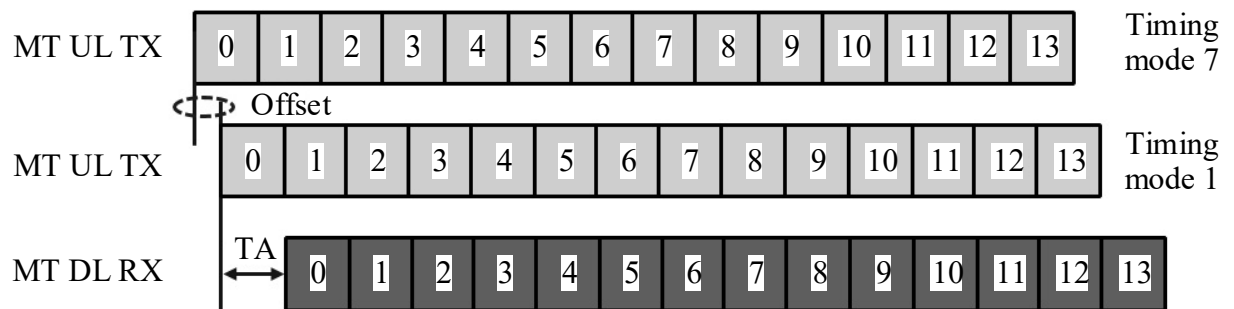


FIG. 17

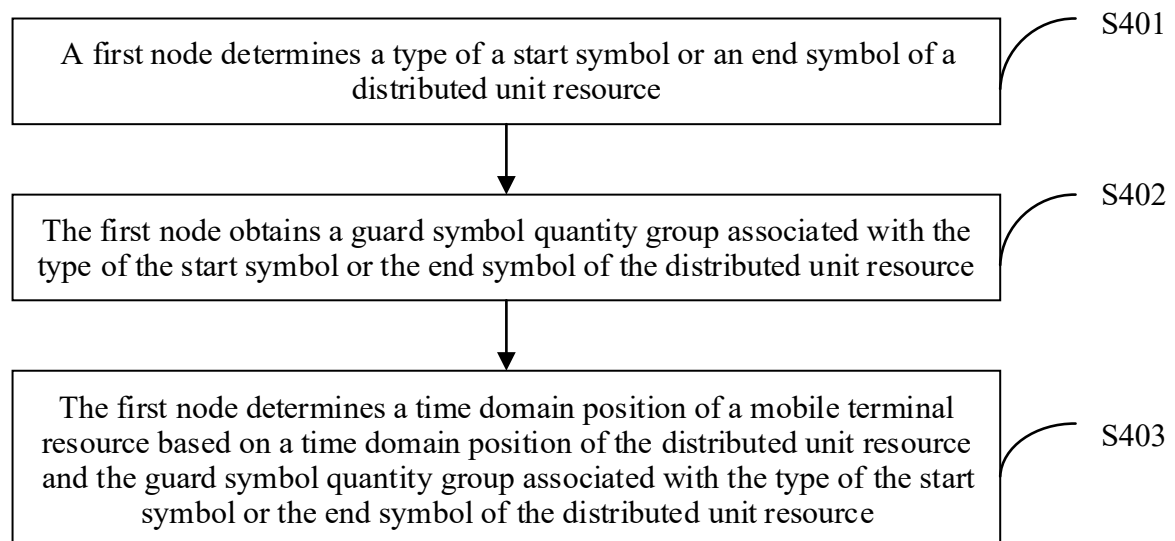


FIG. 18

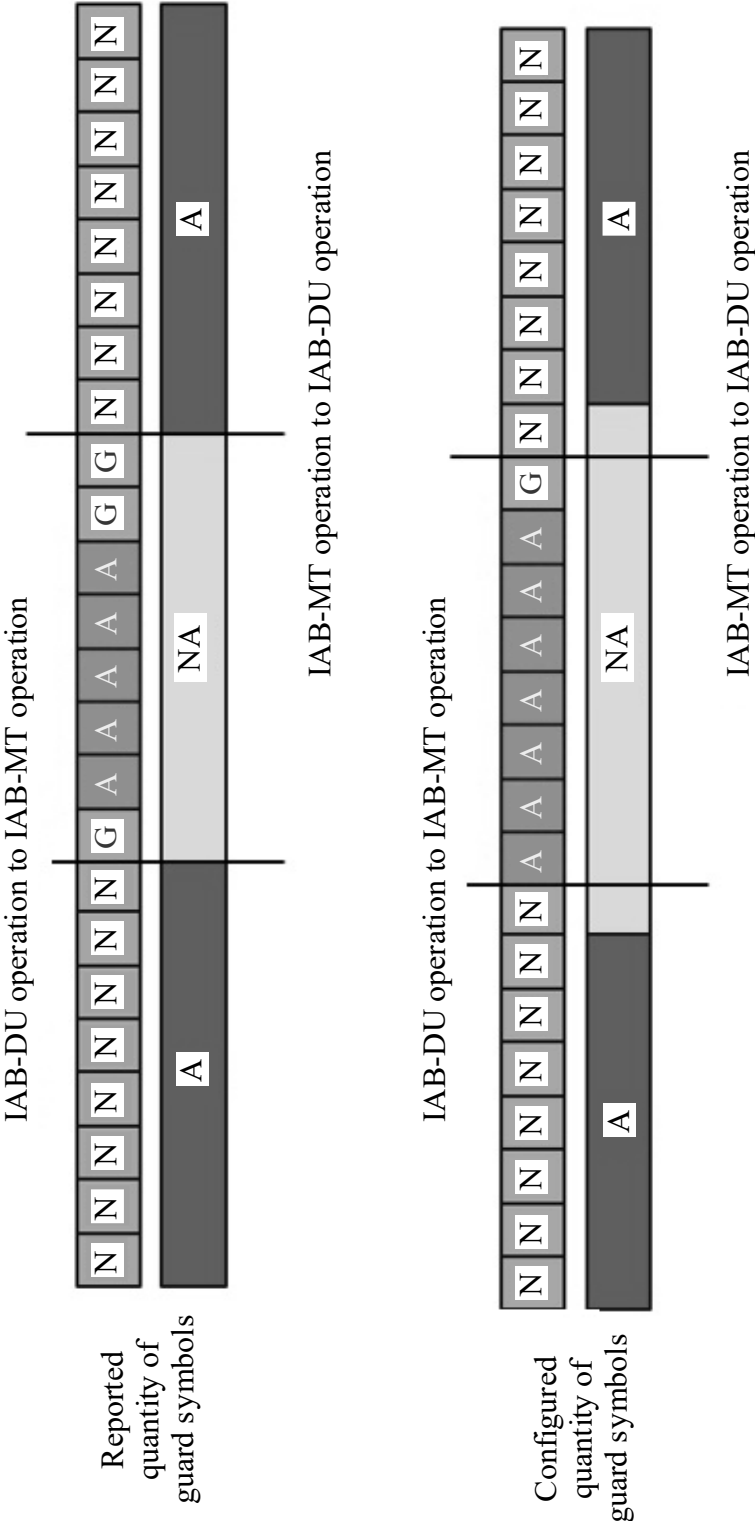


FIG. 19

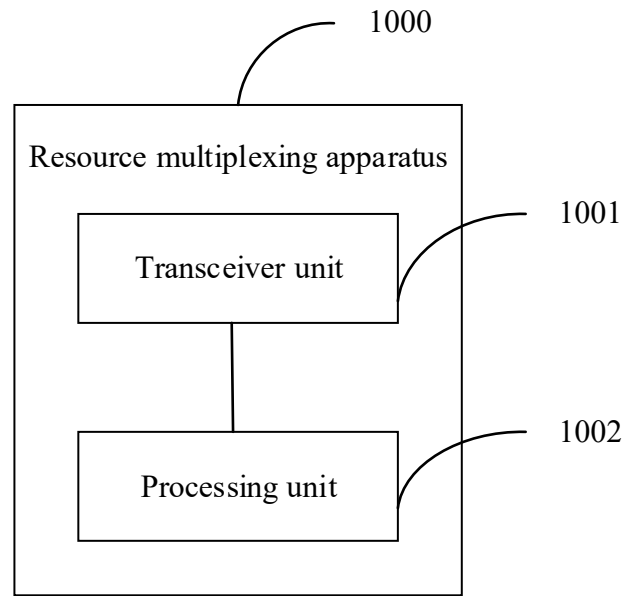


FIG. 20

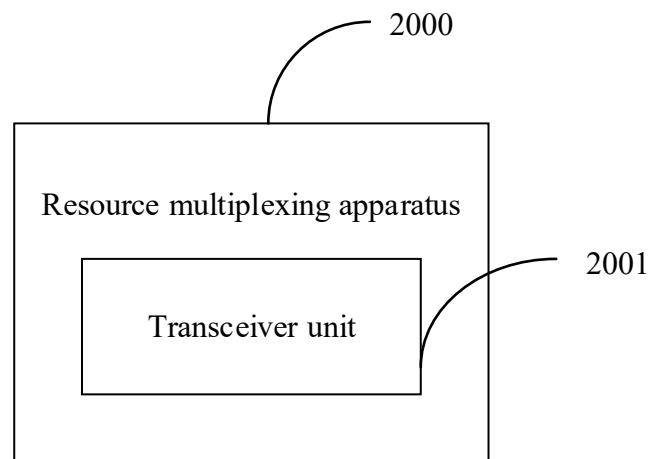


FIG. 21

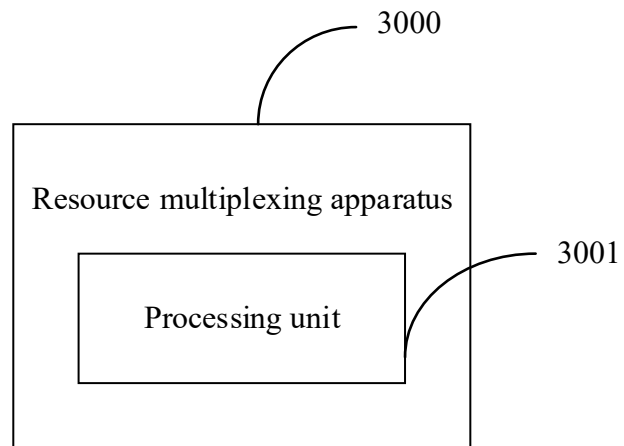


FIG. 22

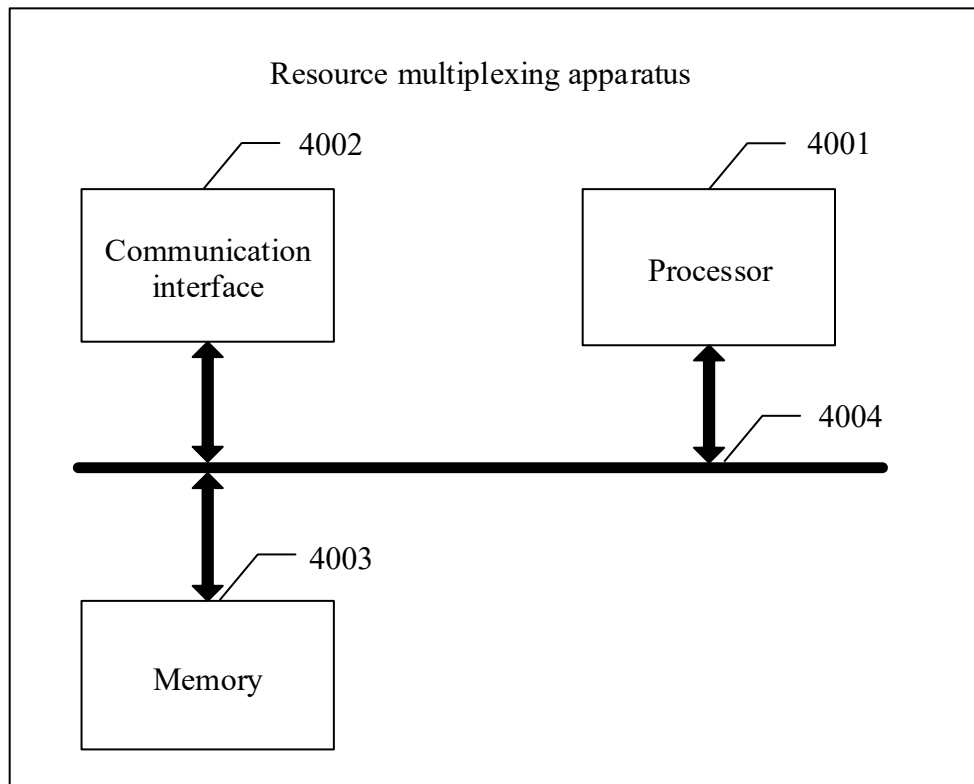


FIG. 23