TESTER FOR INTEGRATED CIRCUITS ON SILICON WAFER

TECHNICAL FIELD

The present invention relates to a method and a device for testing integrated circuits disposed on a silicon wafer.

PRIOR ART

Integrated circuits are manufactured on silicon wafers. A silicon wafer comprises a large number of integrated circuits, typically thousands. The testers used for testing integrated circuits comprise a limited number of input/output connections with the silicon wafer that cannot be increased.

To test all the integrated circuits on a silicon wafer, the tester comes into contact by means of a probe card with rectangular zones of the integrated circuit several times in order to establish an electrical connection with the integrated circuit. A plurality of integrated circuits are tested simultaneously in order to reduce the time for testing the silicon wafer.

The larger the number of integrated circuits tested in parallel, the shorter the time for testing the silicon wafer. The larger the number of test probes used for testing an integrated circuit, the fewer the number of integrated circuits tested in parallel because of the limitation imposed by the number of input/output connections and of test probes of the tester.

The aim of the present invention is to solve the drawbacks of the prior art by proposing a test method and devices wherein only the connections used for supplying electrical energy to the integrated circuits are used during the testing of an integrated circuit.

DISCLOSURE OF THE INVENTION

For this purpose, according to a first aspect, the invention proposes a tester for integrated circuits on a silicon wafer, characterised in that the tester comprises two connections for supplying electrical energy to an integrated circuit, characterised in that the tester comprises:

- means for measuring a first current delivered to the integrated circuit,

- means for transmitting a message to the integrated circuit, the message being transmitted while modulating the amplitude of the supply voltage of the integrated circuit by a predetermined binary sequence, said predetermined sequence representing a command for configuring a communication interface of the integrated circuit, the communication interface being connected to the two connections,

- means for measuring a second current delivered to the integrated circuit,

- means for calculating, from the currents measured, information for testing the integrated circuit.

The invention also relates to a method for testing integrated circuits on a silicon wafer, characterised in that a tester comprises two connections for supplying electrical energy to an integrated circuit, characterised in that the method is performed by the tester and comprises the steps of:

- measuring a first current delivered to the integrated circuit,

- transmitting a message to the integrated circuit, the message being transmitted while modulating the amplitude of the supply voltage of the integrated circuit by a predetermined binary sequence, said predetermined sequence representing a command to configure a communication interface of the integrated circuit, the communication interface being connected to the two connections,

- measuring a second current delivered to the integrated circuit,

- calculating, from the currents measured, information for testing the integrated circuit.

Thus, by using only the power-supply connections of the integrated circuit for testing the integrated circuit, the number of integrated circuits tested in parallel is increased. The time for testing the integrated circuits of a silicon wafer is reduced and the cost of producing the integrated circuits is reduced.

According to a particular embodiment of the invention, the means for measuring the first current delivered to the integrated circuit are activated prior to the transfer of the message to the integrated circuit and the means for measuring the second current delivered

to the integrated circuit are activated after the transfer of the message to the integrated circuit.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for obtaining an electrical voltage in the integrated circuit and the information calculated is the electrical voltage in the integrated circuit.

Thus the tester can check whether the electrical voltage complies with a specification and if not being able to adjust it from a specific command without the use of a supplementary connection and by taking the elements already present in the integrated circuit.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for obtaining an electrical current in the integrated circuit and the information calculated is the electrical current in the integrated circuit.

Thus the tester can check whether the electrical current complies with a specification and if not being able to adjust it using a specific command without the use of a supplementary connection and by taking the elements already present in the integrated circuit.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for transmitting a reference voltage to the integrated circuit, the configuration command comprising a coefficient to be applied by the integrated circuit to the supply voltage of the integrated circuit and the information calculated is a voltage for checking whether the reference voltage has been applied.

Thus the tester can adjust a reference voltage using a specific command without the use of a supplementary connection and by taking the elements already present in the integrated circuit.

According to a particular embodiment of the invention, the means for measuring the first and the second current delivered to the integrated circuit are activated after the

message is transferred to the integrated circuit and the current measurements being spaced apart by a predefined period.

The invention also relates to an integrated circuit comprising two connections for supplying electrical energy to the integrated circuit, characterised in that the integrated circuit comprises:

- means for receiving a message comprising a configuration command sent by the tester, the message being a predetermined binary sequence amplitude modulating the supply voltage of the integrated circuit,
- means for configuring a communication interface of the integrated circuit according to the configuration command by positioning a switch of the communication interface in a closed position, the communication interface being connected to the two connections.

The invention also relates to a method for testing an integrated circuit comprising two connections for supplying electrical energy to the integrated circuit, characterised in that the method is executed by the integrated circuit and comprises the steps of:

- receiving a message comprising a configuration command sent by a tester, the message being a predetermined binary sequence amplitude modulating the supply voltage of the integrated circuit,
- configuring a communication interface of the integrated circuit according to the configuration command by positioning a switch of the communication interface in a closed position, the communication interface being connected to the two connections.

Thus, by using only the power-supply connections of the integrated circuit for testing the integrated circuit, the number of integrated circuits tested in parallel is increased. The time for testing the integrated circuits of a silicon wafer is reduced and the cost of reducing the integrated circuits is reduced.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for supplying a value of an electrical voltage in the integrated circuit.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for supplying a value of an electrical current in the integrated circuit.

According to a particular embodiment of the invention, the command for configuring the communication interface of the integrated circuit is a command for receiving a reference voltage of the tester, the configuration command comprising a coefficient, and the integrated circuit further comprises:

- means for applying a voltage divider bridge or a charge pump between the two connections;
- means for positioning another switch of the communication interface in a closed position.

The invention also relates to the computer programs stored on an information carrier, said programs comprising instructions for implementing the methods previously described, when they are loaded into and executed by a computer system.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention mentioned above, as well as others, will emerge more clearly from the reading of the following description of an example embodiment, said description being made in relation to the accompanying drawings, among which:

[Fig. 1] shows a system for testing integrated circuits on a silicon wafer;

[Fig. 2] shows an architecture of a test device according to the present invention;

[Fig. 3] shows an architecture of an integrated circuit on a silicon wafer according to the present invention;

[Fig. 4] shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for obtaining a value of a voltage in the integrated circuit;

[Fig. 5] shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for obtaining a value of a current in the integrated circuit;

[Fig. 6] shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for transmitting a value of a voltage to the integrated circuit;

[Fig. 7] shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for checking the correct transmission of a value of a voltage in the integrated circuit;

[Fig. 8a] shows an example of an algorithm executed by the tester for obtaining a value of a voltage in the integrated circuit;

[Fig. 8b] shows an example of an algorithm executed by the integrated circuit for transmitting a value of a voltage in the integrated circuit;

[Fig. 9a] shows an example of an algorithm executed by the tester for obtaining a value of a current in the integrated circuit;

[Fig. 9b] shows an example of an algorithm executed by the integrated circuit for transmitting a value of a current in the integrated circuit;

[Fig. 10a] shows an example of an algorithm executed by the tester for transmitting a set voltage value to the integrated circuit;

[Fig. 10b] shows an example of an algorithm executed by the integrated circuit for receiving a set voltage value in the integrated circuit.

DETAILED DISCLOSURE OF EMBODIMENTS

Fig. 1 shows a system for testing integrated circuits on a silicon wafer.

In Fig. 1 a tester Te tests the integrated circuits CI of a silicon wafer DUT by means of a plurality of probe cards coming into contact with the rectangular zones of a group of integrated circuits that are tested in parallel.

The tester Te is for example a computer that controls one or more probe cards. The tester Te tests whether the integrated circuits comply with a specification and enables parameters of the integrated circuits to be adjusted.

According to the present invention, each integrated circuit has two contact zones, represented respectively by a black square in Fig. 1, which are used both for testing the

integrated circuit and for powering the integrated circuit CI. When two probes are in contact with the two contact zones, the integrated circuit is supplied with electrical energy and an input/output connection is made according to the present invention.

In Fig. 1, an integrated circuit is tested by means of a probe card comprising the probes Cap1 and Cap2. Naturally a large number of integrated circuits are tested in parallel, the example in Fig. 1 being merely a simplification of actual conditions.

Likewise, only seven integrated circuits are shown in Fig. 1 for reasons of simplification. Naturally a larger number of integrated circuits are present on the silicon wafer DUT.

Using the two energy-supply contact zones for testing the integrated circuit according to the present invention is possible by virtue of a protocol for communicating between the tester Te and each integrated circuit CI so that the tester Te can indicate the type of configuration that must be made and so that the integrated circuit CI understands same. The same applies to the exchange of information between the integrated circuit CI and the tester Te.

In testing an integrated circuit, both digital and analogue signals are exchanged between the integrated circuit CI and the tester Te. For example, adjusting parameters of the flash memory of the integrated circuit CI and selecting certain test modes of the flash memory make it possible to measure electrical voltages and/or currents.

Fig. 2 shows an architecture of a test device or tester according to the present invention.

The tester Te comprises:

- a processor, microprocessor or microcontroller 200;
- a volatile memory 203;
- a ROM memory 202;
- a communication interface 205 that comprises at least one probe card;
- a communication bus 201 connecting the processor 200 to the ROM memory 202, to the RAM memory 203 and to the interface 205.

The processor 200 is capable of executing instructions loaded in the volatile memory 203 from the ROM memory 202, from an external memory (not shown) or from a storage medium. When the tester Te is powered up, the processor 200 is capable of reading instructions from the volatile memory 203 and executing them. These instructions form a computer program that causes the implementation, by the processor 200, of all or part of the method described in relation to Figs. 8a, 9a and 10a.

All or some of the methods described in relation to Figs. 8a, 9a and 10a may be implemented in software form by executing a set of instructions by a programmable machine, such as a DSP (digital signal processor) or a microcontroller or be implemented in hardware form by a machine or a dedicated component, such as an FPGA (field-programmable gate array) or an ASIC (application-specific integrated circuit).

Fig. 3 shows an architecture of an integrated circuit on a silicon wafer according to the present invention.

The integrated circuit Te comprises:

- a processor, microprocessor or microcontroller 300;
- a volatile memory 303;
- a ROM memory 302;
- a flash memory 304;
- a communication interface 305;
- a communication bus 301 connecting the processor 300 to the ROM memory 302, to the RAM memory 303, to the flash memory 304 and to the interface 305.

The processor 300 is capable of executing instructions loaded in the volatile memory 303 from the ROM memory 302. When the integrated circuit CI is powered up, the processor 300 is capable of reading instructions from the volatile memory 303 and executing them. These instructions form a computer program that causes the implementation, by the processor 300, of all or some of the methods described in relation to Figs. 8b, 9b and 10b.

All or some of the methods described in relation to Figs. 8b, 9b and 10b may be implemented in software form by executing a set of instructions by a programmable

machine, such as a DSP (digital signal processor) or a microcontroller or be implemented in hardware form by a machine or a dedicated component.

Fig. 4 shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for obtaining a value of a voltage in the integrated circuit.

The communication interface 205 of the tester Te comprises a voltage source Vt that supplies the electrical energy to the integrated circuit 305 by means of the contact probes Cap1 and Cap2.

A first termination of the voltage source Vt is connected to the contact probe Cap2 and a second termination of the voltage source Vt is connected to a first termination of a means for measuring the current Icc delivered to the integrated circuit CI and to a first termination of a switch SWT.

A second termination of the means for measuring the current Icc delivered to the integrated circuit CI is connected to a second termination of the switch SWT.

The tester Te generates messages intended for the integrated circuit CI in the form of binary data that modulate the voltage of the voltage source Vt. When the messages are transferred, the switch SWT connects the second termination of the voltage source Vt to the contact probe Cap1 and when a voltage or current value is obtained or when a value of a voltage is transmitted to the integrated circuit, the second termination of the current-measuring means Icc is connected to the contact probe Cap1.

When a value of a voltage in the integrated circuit CI is obtained, the communication interface 305 of the integrated circuit CI is configured to have, between the contact probes Cap1 and Cap2, a variable voltage source Vc, a switch SWC1 and two resistors R and R2.

A resistor R1 represents the load of the integrated circuit CI between the contact probes Cap1 and Cap2 when it is in a conventional operating mode.

In other words, the current I1 passing through the resistor R1 is the current consumed by the integrated circuit in the conventional operating mode supplied by a voltage Vcc.

A first termination of the resistor R1 is connected to the contact probe Cap1 and to a first termination of the voltage source Vc. A second termination of the voltage Vc is connected to a first termination of the switch SWC1 and to a first termination of the resistor R2.

The voltage Vc represents the internal voltage for supplying the transistors and the RAM and flash memories of the integrated circuit. The resistor R2 represents the load associated with this voltage source Vc. The current consumed by the integrated circuit therefore represents the sum of the currents I1 and I2.

A second termination of the switch SWC1 is connected to a first termination of the resistor R.

A second termination of the resistor R is connected to a second termination of the resistor R2 and to the contact probe Cap2.

The current circulating in the resistor R2 is denoted I2 and the current in the resistor R is denoted I3. The voltage V1 at the terminals of the resistor R2 is the voltage the value of which is obtained.

Fig. 5 shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for obtaining a value of a current in the integrated circuit.

The communication interface 205 of the tester Te is identical to that described with reference to Fig. 4.

When a value of a current in the integrated circuit CI is obtained, the communication interface 305 of the integrated circuit CI is configured to have, between the contact probes Cap1 and Cap2, a voltage source Vc, a switch SWC2, a current source Ic and a resistor R2.

The resistor R1 represents, as described with reference to Fig. 4, the load of the integrated circuit CI between the contact probes Cap1 and Cap2 when it is in a conventional operating mode supplied by a voltage Vcc.

The voltage Vc represents the internal voltage for supplying the transistors and the RAM and flash memories of the integrated circuit. The resistor R2 represents the load

associated with this voltage source Vc. The current consumed by the integrated circuit therefore represents the sum of the currents I1 and I2.

A first termination of the resistor R1 is connected to the contact probe Cap1, to a first termination of the variable voltage source Vc and to a first termination of the current source. A second termination of the voltage source Vc is connected to a first termination of the resistor R2.

A second termination of the current source Ic is connected to a first termination of the switch SWC2.

A second termination of the switch SWC2 is connected to a second termination of the resistor R2 and to the contact probe Cap2.

The current circulating in the resistor R2 is denoted I2. The current I4 delivered by the current source Ic is the current the value of which is obtained.

Fig. 6 shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for transmitting a value of a voltage to the integrated circuit.

The communication interface 205 of the tester Te is identical to that described with reference to Fig. 4.

When a value of a reference voltage is transmitted to the integrated circuit CI, the communication interface 305 of the integrated circuit CI is configured to have, between the contact probes Cap1 and Cap2, a voltage source Vc, a switch SWC4, a resistor R2, a charge pump or a voltage divider bridge PC/PD and a resistor R3.

The resistor R1 represents, as described with reference to Fig. 4, the load of the integrated circuit CI between the contact probes Cap1 and Cap2 when it is in a conventional operating mode supplied by a voltage Vcc.

The voltage Vc represents the internal voltage for supplying the transistors and the RAM and flash memories of the integrated circuit. The resistor R2 represents the load associated with this voltage source Vc. The current consumed by the integrated circuit therefore represents the sum of the currents I1 and I2.

A first termination of the switch SWC4 is connected to the contact probe Cap1. A second termination of the switch SWC4 is connected to a first termination of the charge pump or of the voltage divider bridge PC/PD. A second termination of the charge pump or of the voltage divider bridge PC/PD is connected to a first termination of the resistor R3. A second termination of the resistor R3 is connected to the contact probe Cap2.

The current circulating in the resistor R3 is denoted I5. The voltage at the terminals of the resistor R3 is denoted V2.

Fig. 7 shows an example of an electrical configuration of the communication interfaces of the tester and of an integrated circuit for checking the correct transmission of a value of a reference voltage in the integrated circuit.

The communication interface 205 of the tester Te is identical to that described with reference to Fig. 4.

When the correct transmission of a value of a voltage in the integrated circuit is verified, the communication interface 305 of the integrated circuit CI is configured to have, between the contact probes Cap1 and Cap2, a voltage source Vc, a switch SWC4, a resistor R2, a charge pump or a voltage divider bridge PC/PD, and a resistor R3 as described in relation to Fig. 6, as well as a switch SWC3, and a resistor R identical to that described with reference to Fig. 4.

A first termination of the switch SWC3 is connected to the second termination of the charge pump or of the voltage divider bridge PC/PD.

The second termination of the switch SWC3 is connected to the first termination of the resistor R, the second termination of the resistor R is connected to the contact probe Cap2.

The current circulating in the resistor R3 is denoted I5 and the current circulating in the resistor R is denoted I6.

The voltage V2 is the voltage at the terminals of the resistor R when the switch SWC3 is closed.

Fig. 8a represents an example of an algorithm executed by the tester for obtaining a value of a voltage in the integrated circuit.

At the step S80, the tester Te obtains, from the means for measuring the current Ic, a first value Icc1 of the current delivered to the integrated circuit C1.

At the step S81, the tester Te demands the transfer of a message intended for the integrated circuit CI indicating to it that a value of an analogue voltage is requested.

The message is transmitted by means of the contact probes Cap1 and Cap2 while modulating the amplitude of the voltage source Vt by a predetermined binary sequence.

At the step S82, the tester Te obtains, from the means for measuring current Icc, a second value Icc2 of the current delivered to the integrated circuit CI.

At the step S83, the tester calculates the value of the analogue voltage requested in accordance with the following formula: V1 = (Icc2 - Icc1)*R where R is the resistance as described with reference to Fig. 4. The value of the resistance R is known and is identical for all the integrated circuits.

Fig. 8b shows an example of an algorithm executed by the integrated circuit for transmitting a value of a voltage in the integrated circuit.

At the step S85, the integrated circuit CI receives from the tester Te a message indicating to it that a value of an analogue voltage is requested.

The message is received by means of the contact probes Cap1 and Cap2 and is amplitude modulated by a predetermined binary sequence. The message is detected using voltage detectors in order to detect two different voltage levels.

At the following step S86, the integrated circuit CI configures the communication interface in the configuration as described in Fig. 4 wherein the switch SWC1 is closed.

Thus the current Icc1 measured by the tester Te is equal to Icc1 = I1 + I2 = VCC/R1 + V1/R2 where VCC is the voltage between the contact probes Cap1 and Cap2.

Thus the current Icc2 measured by the tester Te is equal to Icc2 = I1 + I2 + I3 = VCC/R1 + V1/R2 + V1/R.

Icc2 - Icc1 = I3 = V1/R and V1 = R*(Icc2 - Icc1).

Fig. 9a shows an example of an algorithm executed by the tester for obtaining a value of a current in the integrated circuit.

At the step S90, the tester Te obtains, from the means for measuring current Ic, a first value Icc1 of the current delivered to the integrated circuit CI.

At the step S91, the tester Te demands the transfer of a message to the integrated circuit CI indicating to it that a value of a current is requested.

The message is transmitted by means of the contact probes Cap1 and Cap2 while modulating the amplitude of the voltage source Vt by a predetermined binary sequence.

At the step S92, the tester Te obtains, from the means for measuring current Ic, a second value Icc3 of the current delivered to the integrated circuit CI.

At the step S93, the tester calculates the value of the current requested in accordance with the following formula: I4 = Icc3 - Icc1.

Fig. 9b shows an example of an algorithm executed by the integrated circuit for transmitting a value of a current in the integrated circuit.

At the step S95, the integrated circuit CI receives from the tester Te a message indicating to it that a value of an analogue voltage is requested.

The message is received by means of the contact probes Cap1 and Cap2 and is amplitude modulated by a predetermined binary sequence. The message is detected using the voltage detectors in order to detect two different voltage levels.

At the following step S96, the integrated circuit CI configures the communication interface in the configuration as described in Fig. 5 wherein the switch SWC2 is closed.

Thus the current Icc1 measured by the tester Te is equal to Icc1 = I1 + I2 = VCC/R1 + V1/R2 where VCC is the voltage between the contact probes Cap1 and Cap2.

Thus the current Icc3 measured by the tester Te is equal to Icc3 = I1 + I2 + I5, I5 = Icc3 - Icc1.

Fig. 10a shows an example of an algorithm executed by the tester for transmitting a set voltage value to the integrated circuit.

At the step S100, the tester Te demands the transfer of a message to the integrated circuit CI indicating to it that a reference voltage value is being sent.

The message comprises information indicating the value of a coefficient denoted coeff.

The message is transmitted by means of the contact probes Cap1 and Cap2 while modulating the amplitude of the voltage source Vt by a predetermined binary sequence.

At the step S101, the tester Te obtains, from the means for measuring the current Ic, a first value Icc4 of the current delivered to the integrated circuit CI.

At the step S102, the tester Te obtains, from the means for measuring the current Ic, a second value Icc5 of the current delivered to the integrated circuit CI. The measurements of the currents are spaced apart by a predefined period equal to the predefined period for example lying between around a hundred microseconds and around ten milliseconds.

At the step S103, the tester calculates the value of the reference voltage in accordance with the following formula: $V2 = R(Icc5 - Icc4)$ and checks whether this is in accordance with the reference voltage.

Fig. 10b shows an example of an algorithm executed by the integrated circuit for receiving a set voltage value in the integrated circuit.

At the step S105, the integrated circuit CI receives from the tester Te a message indicating to it that a value of a reference voltage is being transmitted.

The message comprises information indicating the value of a coefficient denoted coeff.

The message is received by means of the contact probes Cap1 and Cap2 and is amplitude modulated by a predetermined binary sequence. The message is detected using the voltage detectors in order to detect two different voltage levels.

At the following step S106, the integrated circuit CI configures the communication interface wherein the switch SWC3 is open and the switch SWC4 is closed, determines that a voltage divider bridge must be applied between the contact probes Cap1 and Cap2 if the value of the coefficient is less than 1 or determines that a charge pump must be applied

between the contact probes Cap1 and Cap2 if the value of the coefficient is greater than 1 and applies the value of the coefficient coeff to the voltage divider bridge or to the charge pump.

Thus the current Icc4 measured by the tester Te is equal to Icc4 = I1 + + I2 + I5 = VCC/R1 + V1/R2 + V2/R3 where VCC is the voltage between the contact probes Cap1 and Cap2.

At the following step S107, the integrated circuit CI configures the communication interface wherein the switch SWC3 is closed.

Thus the current Icc5 measured by the tester Te is equal to Icc5 = I1 + I2 + I5 + I6, V2 = R(Icc5 - Icc4).

CLAIMS

1. A system comprising a tester for integrated circuits on a silicon wafer, and an integrated circuit, characterised in that the tester comprises two connections for supplying electrical energy to an integrated circuit, and in that the system comprises:

means (Icc), included in the integrated-circuit tester, for measuring a first current delivered to the integrated circuit,

means (Vt), included in the integrated-circuit tester, for transmitting a message to the integrated circuit, the message being transmitted while modulating the amplitude of a supply voltage of the integrated circuit by a predetermined binary sequence, the predetermined binary sequence representing a command for configuring a communication interface of the integrated circuit, the communication interface being connected to the two connections,

means, included in the integrated circuit, for receiving the message, the message indicating that an analogue voltage value is requested or a current value is requested or that a reference voltage is transmitted,

means, included in the integrated circuit, for configuring the communication interface of the integrated circuit according to the configuration command by positioning a switch of the communication interface in a closed position, the communication interface being connected to the two connections and, when the switch of the communication interface is in the closed position, a part of the first current delivered to the integrated circuit passes through a resistor when the message indicates that an analogue voltage value is requested, or a current source is connected to the two connections when the message indicates that a current value is requested or a resistor in series with a charge pump or a voltage divider bridge are connected to the two connections when the message indicates that a reference voltage is being transmitted,

means (Icc), included in the integrated-circuit tester, for measuring a second current delivered to the integrated circuit,

means, included in the integrated-circuit tester, for calculating, from the measured currents, information for testing the integrated circuit.

2. A system according to Claim 1, characterised in that the means for measuring the first current delivered to the integrated circuit are activated prior to the transfer of the message to the integrated circuit and the means for measuring the second current delivered to the integrated circuit are activated after the transfer of the message to the integrated circuit.

3. A system according to Claim 1, characterised in that, when the command for configuring the communication interface of the integrated circuit is a command for obtaining the analogue voltage value in the integrated circuit, the information calculated is the electrical voltage in the integrated circuit.

4. A system according to Claim 1, characterised in that, when the command for configuring the communication interface of the integrated circuit is a command for obtaining the current value in the integrated circuit, the information calculated is the electrical current in the integrated circuit.

5. A system according to Claim 1, characterised in that, when the command for configuring the communication interface of the integrated circuit is a command for transmitting a reference voltage to the integrated circuit, the configuration command comprises a coefficient to be applied by the integrated circuit to the supply voltage of the integrated circuit and the information calculated is a voltage for checking whether the reference voltage has been applied.

6. A system according to Claim 5, characterised in that the means for measuring the first and second current delivered to the integrated circuit are activated after the transfer of the message to the integrated circuit and the measurements of the currents being spaced apart by a predefined period.

7. A method for testing integrated circuits on a silicon wafer, characterised in that a tester comprises two connections for supplying electrical energy to the integrated circuit, characterised in that the method comprises the steps of:

measuring, by the integrated-circuit tester, a first current delivered to the integrated circuit,

transmitting, by the integrated-circuit tester, a message to the integrated circuit, the message being transmitted while modulating the amplitude of a supply voltage of the integrated circuit by a predetermined binary sequence, the predetermined binary sequence representing a command for configuring a communication interface of the integrated circuit, the communication interface being connected to the two connections,

receiving, by the integrated circuit, the message comprising the configuration command sent by the tester, the message being the predetermined binary sequence amplitude modulating the supply voltage of the integrated circuit, the message indicating that an analogue voltage value is requested or a current value is requested or that a reference voltage is transmitted,

configuring, by the integrated circuit, the communication interface of the integrated circuit according to the configuration command by positioning a switch of the communication interface in a closed position, the communication interface being connected to the two connections and, when the switch of the communication interface is in the closed position, a part of the first current delivered to the integrated circuit passes through a resistor when the message indicates that an analogue voltage value is requested, or a current source is connected to the two connections when the message indicates that a current value is requested or a resistor in series with a charge pump or a voltage divider bridge are connected to the two connections when the message indicators that a reference voltage is transmitted,

measuring, by the integrated-circuit tester, a second current delivered to the integrated circuit,

calculating, by the integrated-circuit tester, from the currents measured, information for testing the integrated circuit.