Description

Title of Invention: DIRECT AC POWER CONVERTER

Technical Field

[0001] The present invention relates to a direct AC power converter, and particularly, to a configuration including a rectifying circuit, an inverter, and a boost chopper.

Background Art

[0002] Patent Documents 1 and 2 and Non-Patent Document 1 introduce direct AC power converters. In each of these direct AC power converters, a boost chopper is used and receives an electric power from a rectifying circuit and supplies the electric power to an inverter so that pulsation of an instantaneous power is reduced.

Prior Art Documents

Patent Documents

[0003] Patent Document 1: Japanese Patent Application Laid-Open No. 2011-193678

Patent Document 2: Japanese Patent Application Laid-Open No. 2012-135184

Patent Document 3: Japanese Patent Application Laid-Open No. 2014-82926

Non-Patent Document

[0004] Non-Patent Document 1: Ohnuma, Itoh, "Experimental Verification of Single Phase to Three Phase Converter Using an Active Buffer circuit with a Charge Circuit", IEEJ 2010 Industry Applications Society Conference 1-124, pp. I-587-590 (2010)

Summary of Invention

Problems to be Solved by the Invention

[0005] In the techniques introduced in Patent Documents 1 and 2 and Non-Patent Document 1, however, a period of charge from the rectifying circuit to the capacitor and a period of discharge from the capacitor to the inverter are set alternately in each 1/4 of a

cycle of an input AC voltage. The magnitude of an output voltage thus remains at $1/\sqrt{2}$ times a crest value of the input AC voltage.

[0006] Also in the technique described in Patent Document 3, a capacitor is unnecessarily charged and discharged in view of the operation of an inverter, so that a boost chopper is likely to require an increased power capacity.

[0007] The present invention therefore has an object to provide a technique of reducing a power capacity required for a boost chopper while increasing a voltage output from a direct AC power converter more than in a conventional technique.

Means to Solve the Problems

[0008] A direct AC power converter according to the present invention includes a DC link (7), a first rectifying circuit (5, 51), a boost chopper (3), and a switch (41).

[0009] The DC link has a first power supply line (L1) and a second power supply line (L2) to which a potential lower than a potential of the first power supply line is applied.

[0010] The first rectifying circuit has a plurality of input terminals that receive an input of an AC voltage, and a pair of output terminals (51c, 51d) each connected to the DC link.

[0011] The inverter converts a voltage applied to the DC link into another multi-phase AC voltage.

[0012] The boost chopper has a capacitor (34) at its output stage.

[0013] The switch switches a discharge and non-discharge from the capacitor to the DC link.

[0014] In a first aspect of the direct AC power converter according to the present invention, in the boost chopper, the capacitor is charged at least during a first period being a part of a period during which a discharge duty (dc) is greater than 0.

[0015] The discharge duty is a time ratio at which the switch is conductive.

[0016] A virtual DC link voltage (Vdc) is greater than or equal to a first value (V1) and

smaller than or equal to a second value (V2). The virtual DC link voltage is expressed as a sum of a product (dc·Vc) of the discharge duty and a voltage between both ends (Vc) of the capacitor and a product (dr·Vrec) of a rectifying duty (dr) and a rectified voltage (Vrec) of the AC voltage.

[0017] The rectifying duty takes a value obtained by subtracting a sum of the discharge duty and a zero voltage duty (dz) from 1.

[0018] The zero voltage duty is a time ratio at which the inverter (6) adopts a zero voltage vector irrespective of magnitude of a voltage output from the inverter (6).

[0019] The first value is a maximum value (max(|Vuv|, |Vvw|, |Vwu|)) among absolute values of respective line-to-line voltages of the multi-phase AC voltage.

[0020] The second value is a maximum value that the absolute values can take.

[0021] In a second aspect of the direct AC power converter according to the present invention, in the first aspect, the capacitor is charged in the boost chopper during the first period and a part or whole of a period at which the discharge duty is 0.

[0022] In a third aspect of the direct AC power converter according to the present invention, in the first or second aspect, the capacitor (34) is charged with a charge power (Pci) and discharged with a discharge power (Pco) during the first period. The first period has a period during which the charge power is greater than the discharge power and a period during which the discharge power is greater than the charge power.

[0023] In a fourth aspect of the direct AC power converter according to the present invention, in any one of the first to third aspects, a period during which the virtual DC link voltage (Vdc) takes the first value (V1) is present.

[0024] In a fifth aspect of the direct AC power converter according to the present invention, in any one of the first to fourth aspects, the discharge duty at which the zero voltage duty (dz) is minimum is set based on a command value (irec*) of a rectified

invention, in any one of the first to ninth aspects, further includes a diode connected in parallel with the switch (41). A forward direction of the diode is a direction in which the capacitor (34) is charged from the DC link (7).

Effects of the Invention

[0031] The capacitor is charged in the boost chopper at least during a part of the period in which the discharge duty is greater than 0, so that an average value of maximum values of voltages that can be output from the inverter in a cycle of control of switching of the inverter can exceed $1/\sqrt{2}$ times a crest value of the AC voltage.

[0032] A small discharge duty can be selected, and thus, the average value or the effective value of the current flowing in the inductor of the boost chopper can be reduced more than in the conventional technique.

[0033] These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0034] FIG. 1 is a circuit diagram illustrating a configuration of a direct AC power converter according to an embodiment;

FIG. 2 is a circuit diagram illustrating another configuration of the direct AC power converter according to the embodiment;

FIG. 3 is a circuit diagram of an equivalent circuit of the direct AC power converter according to the embodiment;

FIG. 4 is a block diagram illustrating a configuration of a controller of the direct AC power converter according to the embodiment;

FIG. 5 is a flowchart summarizing steps of obtaining a rectifying duty, a zero

voltage duty, a discharge duty, and a current command value;

FIGS. 6 and 7 are graphs showing waveforms of specifications of Example 1;

FIGS. 8 and 9 are graphs showing waveforms of specifications of Example 2;

FIG. 10 is a graph showing a relationship between a command value of a virtual DC link voltage and a command value of an inverter;

FIG. 11 is a graph showing a relationship between a command value of the virtual DC link voltage and a command value of the inverter;

FIGS. 12 and 13 are graphs showing waveforms of specifications of Example 3;

FIG. 14 is a graph showing waveforms of currents flowing in inductors of Examples 2 and 3;

FIG. 15 is a graph showing waveforms of currents flowing through capacitors of Examples 2 and 3;

FIG. 16 is a graph showing an operation of an inverter of Example 2; and

FIG. 17 is a graph showing an operation of an inverter of Example 3.

Description of Embodiments

[0035] FIG. 1 is a circuit diagram illustrating a configuration of a direct AC power converter according to an embodiment.

[0036] The direct AC power converter includes a DC link 7, rectifying circuits 51 and 52, a boost chopper 3, a switch 41, and an inverter 6.

[0037] The DC link 7 has power supply lines L1 and L2. A potential lower than the potential of the power supply line L1 is applied to the power supply line L2.

[0038] The rectifying circuit 51 has input terminals 51a and 51b that receive an AC voltage Vin and a pair of output terminals 51c and 51d respectively connected to the power supply lines L1 and L2. The rectifying circuit 51 is of a full-wave rectification type. Illustrated herein is a case in which the rectifying circuit 51 is formed by a diode bridge.

[0039] FIG. 1 illustrates a state in which the AC voltage Vin is supplied to the rectifying circuit 51 from a single-phase AC power supply via a filter circuit 2. The filter circuit 2, however, is provided to cut off a harmonic noise, and thus, a cutoff frequency of the harmonic noise is higher than the frequency of the AC voltage Vin. The function of the filter circuit 2 has hardly any influence on the operations of the respective sections described below, and accordingly, description will be given below without consideration of the operation of the filter circuit 2.

[0040] An operation of the switch 41 and switching operations of the boost chopper 3 and the inverter 6 are controlled by a controller 9. The controller 9 can be regarded as being included in the direct AC power converter as well.

[0041] The inverter 6 converts the voltage applied to the DC link 7 into another multi-phase AC voltage. Illustrated herein is a configuration in which the inverter 6 outputs a three-phase AC voltage to a permanent-magnet synchronous motor PMSM that serves as an inductive load. The inverter 6 is a voltage-source inverter that operates under instantaneous spatial vector control, and may have a publicly known configuration. The inverter 6 outputs a three-phase current Iinv to the permanent-magnet synchronous motor PMSM.

[0042] The boost chopper 3 has a capacitor 34 at its output stage. More specifically, a rectified voltage Vrec of the AC voltage Vin is applied to the boost chopper 3. The rectified voltage Vrec is generated by the rectifying circuit 52 of full-wave rectification type.

[0048] A diode, a forward direction of which is the direction from the DC link 7 toward the boost chopper 3 (more specifically, from the power supply line L1 toward the capacitor 34), is desirably provided to charge the capacitor 34 with a regenerative current from the inverter 6.

[0049] The controller 9 receives an AC voltage Vin (more accurately, a signal indicating its waveform: the same applies to the following), a current Iinv output from the inverter 6, and a capacitor voltage Vc, and outputs control signals Sb, Sc, and Sg. The control signal Sg is a signal for controlling switching of the inverter 6. Since illustrated herein is a case in which the inverter 6 outputs a three-phase voltage, the control signal Sg is a group composed of 6 (= 3 × 2) signals.

[0050] FIG. 2 is a circuit diagram illustrating another configuration of the direct AC power converter according to the embodiment. In comparison with the configuration shown in FIG. 1, the rectifying circuit 51 also serves as the rectifying circuit 52. That is to say, the pair of output terminals 51c and 51d of the rectifying circuit 5 are connected to an input side of the boost chopper 3. In this case, a rectified voltage Vrec is not always applied to the boost chopper 3, unlike the configuration shown in FIG. 1. This is because the other end of the inductor 32 is connected via the power supply line L1 to the switch 41, and depending on an operating status of the switch 41, the capacitor voltage Vc is applied to the boost chopper 3.

[0051] However, FIGs. 1 and 2 can be treated equivalently in an equivalent circuit described below, and thus, a control method described below is common. The equivalent circuit will be described first.

[0052] FIG. 3 is a circuit diagram of the equivalent circuit of each of the direct AC power converters shown in FIGs. 1 and 2. The rectified voltage Vrec is expressed as a voltage source, and accordingly, a switch Grec indicates whether the rectifying circuit 51

than or equal to a value determined by Expression (11), and is thus considered to be set to a minimum value thereof. That is to say, it can be regarded that the discharge duty dc to make the zero voltage duty dz minimum is set also in the discharge zone as in the charge zone and the charge and discharge zone.

[0111] When the rectifying duty dr, the zero voltage duty dz, the discharge duty dc, and the command value ib* are determined in the manner above, the control signals Sb, Sc, and Sg can be generated using a known technique.

[0112] FIG. 4 is a block diagram illustrating a configuration of the controller 9. The controller 9 is roughly divided into a current command generator 91, a DC current (idc) estimator 92, a duty divider 93, a pulse width modulation (PWM) signal generator 94, and a chopper signal generator 95.

[0113] The current command generator 91 generates the command value irec* of the rectified current irec. Although FIG. 4 illustrates a configuration in which the command value irec* has an absolute value of a sinusoidal waveform as described below, the command value irec* is not always limited to providing such a waveform.

[0114] The DC current estimator 92 obtains the estimated value idc^ of the DC current idc. As is understood from the equivalent circuit of FIG. 3, an actual circuit has no portion that can actually measure the DC current idc. Therefore, the estimated value idc^ is adopted in the computations represented by Expressions (6) and (8).

[0115] An electric power to be output from the inverter 6 can be obtained in the equivalent circuit from the DC current idc and the virtual DC link voltage Vdc. In contrast, an electric power to be output from the inverter 6 in an actual circuit is obtained from a three-phase current Iinv and a three-phase voltage Vinv to be output from the inverter 6. Therefore, theoretically, the estimated value idc^ can be obtained from the virtual DC link voltage Vdc, the current Iinv, and the voltage Vinv.

[0116] It is noted that the voltage Vinv to be output from the inverter 6 is controlled by the pulse width modulation signal generator 94 to follow its command value Vinv*. The virtual DC link voltage Vdc cannot be measured per se, but is controlled by the duty divider 93 to follow the command value Vdc*. The current Iinv can be measured from wire connection between the inverter 6 and the permanent-magnet synchronous motor PMSM. In this embodiment, therefore, the estimated value idc^ is obtained from the command values Vdc* and Vinv* and the current Iinv. Needless to say, the estimated value idc^ may be obtained by another method.

[0117] The duty divider 93 determines the rectifying duty dr, the zero voltage duty dz, the discharge duty dc, and the command value ib* in accordance with the methods described in the first to third cases on the basis of the command values Vdc* and irec*, the capacitor voltage Vc, the rectified voltage Vrec, and the estimated value idc^. The expression "duty 'divider'" is given here because as represented by Expression (2), a value 1 is divided by the rectifying duty dr, the zero voltage duty dz, and the discharge duty dc.

[0118] The pulse width modulation signal generator 94 generates the control signals Sc and Sg on the basis of the rectifying duty dr, the zero voltage duty dz, the discharge duty dc, and the command values Vinv* and Vdc*. For example, these duties and respective phase portions of the command value Vinv* are operated to generate signal waves, and the signal waves can be compared to a triangular carrier to generate the control signals Sc and Sg. Since such a method is publicly known and is described in, for example, Patent Documents 1 and 2, detailed description thereof will be omitted.

[0119] The chopper signal generator 95 has a boost chopper duty arithmetic unit 951 and a pulse width modulation (PWM) signal generator 952. The boost chopper duty arithmetic unit 951 determines the boost duty db on the basis of the command value ib*, the capacitor voltage Vc, and the rectified voltage Vrec.

[0120] A method for determining the boost duty db differs depending on a mode in which the boost chopper 3 operates. The method may be a normal method for determining the discharge duty of a boost chopper, and thus, detailed description thereof will be omitted.

[0121] The pulse width modulation signal generator 952 can also generate the control signal Sb from the boost duty db by a known modulation method.

[0122] A configuration of the current command generator 91 will now be described. The current command generator 91 has an output power (Pout) estimator 911, a trigonometric function value generator 912, a capacitor voltage controller 913, an adder 914, a multiplier 915, and a divider 916.

[0123] The output power estimator 911 obtains an estimated value Pout^ of an output power Pout based on the command value Vinv* and the current Iinv. The DC current estimator 92, which obtains the estimated value idc^ as described above, may receive inputs of the estimated value Pout^ obtained from the output power estimator 911 and the command value Vdc* so as to obtain the estimated value idc^.

[0124] The capacitor voltage controller 913 obtains a deviation Vc* - Vc between the capacitor voltage Vc and its command value Vc* and performs at least proportional control on the deviation Vc* - Vc, then outputting the deviation Vc* - Vc to the adder 914.

[0125] The adder 914 adds an output from the capacitor voltage controller 913 to the estimated value Pout^. This is a process for suitably setting a command value Pin* of the input power by correcting the estimated value Pout^ to be greater/smaller when the capacitor voltage Vc becomes smaller/greater than the command value Vc*, thus reducing the deviation. For stability of the deviation, the capacitor voltage controller 913 desirably adopts not mere proportional control itself but proportional-integral control

smaller discharge duty means a smaller current ic.

[0170] Further, Step S109 processed after Step S107 will also be considered. As described above, the rectifying duty dr becomes greater as the command value Vdc* is smaller. The output power Pout is made constant, and accordingly, the pulsation of the command value Vdc* causes the DC current idc to pulsate. Specifically, the DC current idc becomes greater as the command value Vdc* is smaller. Thus, both the rectifying duty dr and the DC current idc are greater as the command value Vdc* is smaller, and the rectified current irec does not depend on the command value Vdc* as a sinusoidal wave, and accordingly, the current ib is small.

[0171] Such reductions in the currents ib and ic contribute to a reduction in the power capacities required for the inductor 32 and the capacitor 34, and accordingly, miniaturization of the inductor 32 and the capacitor 34, cost reduction, and an improvement in efficiency owing to a reduced calorific value, and further contribute to a reduction in the power capacity required for the boost chopper 3.

[0172] Specifically, the command value Vdc* may be the greatest command value among the command values Vu*, Vv*, and Vw* with respect to a minimum phase. This is because while the inverter 6 cannot output a large voltage exceeding the virtual DC link voltage Vdc, it suffices that the virtual DC link voltage Vdc is the greatest command value among the command values Vu*, Vv*, and Vw* with respect to a minimum phase.

[0173] That is to say, the command value Vdc* may have V1 = max(Vu*, Vv*, Vw*) - min(Vu*, Vv*, Vw*), where a symbol "max()" represents the greatest one among the elements within a parenthesis, and a symbol "min()" represents the smallest one among the elements within a parenthesis.

[0174] Under normal control, phase voltages Vu, Vv, and Vw output from the inverter 6 respectively match the command values Vu*, Vv*, and Vw*, and thus, the value V1 can be obtained

CLAIMS

1. A direct AC power converter comprising:

a DC link having

a first power supply line, and

a second power supply line to which a potential lower than a potential of said first power supply line is applied;

a first rectifying circuit having

a plurality of input terminals that receive an input of an AC voltage, and

a pair of output terminals each connected to said DC link;

an inverter that converts a voltage applied to said DC link into another multi-phase AC voltage;

a boost chopper having a capacitor in an output stage thereof; and

a switch that switches a discharge and non-discharge from said capacitor to said DC link,

wherein

in said boost chopper, said capacitor is charged at least during a first period being a part of a period during which a discharge duty is greater than 0, said discharge duty being a time ratio at which said switch is conductive,

a virtual DC link voltage is greater than or equal to a first value and smaller than or equal to a second value, said virtual DC link voltage being expressed as a sum of a product of said discharge duty and a voltage between both ends of said capacitor and a product of a rectifying duty and a rectified voltage of said AC voltage,

said rectifying duty takes a value obtained by subtracting a sum of said

discharge duty and a zero voltage duty from 1,

said zero voltage duty is a time ratio at which said inverter adopts a zero voltage vector irrespective of magnitude of a voltage output from said inverter,

said first value is a maximum value among absolute values of respective line-to-line voltages of said multi-phase AC voltage, and

said second value is a maximum value that said absolute values are capable of taking.

2. The direct AC power converter according to claim 1, wherein said capacitor is charged in said boost chopper during said first period and a part or whole of a period at which said discharge duty is 0.

3. The direct AC power converter according to claim 1 or 2, wherein

said capacitor is charged with a charge power and discharged with a discharge power during said first period, and

said first period has a period during which said charge power is greater than said discharge power and a period during which said discharge power is greater than said charge power.

4. The direct AC power converter according to any one of claims 1 to 3, wherein a period during which said virtual DC link voltage takes said first value is present.

5. The direct AC power converter according to any one of claims 1 to 4, wherein said discharge duty at which said zero voltage duty is minimum is set based

on a command value of a rectified current being a sum of a current flowing in said boost chopper and a current flowing from said first rectifying circuit to said inverter, a command value of said virtual DC link voltage, a voltage between both ends of said capacitor, said rectified voltage, and a current input to said inverter.

6. The direct AC power converter according to claim 5, wherein

when said virtual DC link voltage is greater than said rectified voltage and said command value of said rectified current is greater than or equal to a product of a predetermined value and a current input to said inverter, said rectifying duty takes said predetermined value, and said discharge duty takes a value obtained by subtracting said predetermined value from 1, and

said predetermined value is a value obtained by dividing a value obtained by subtracting said voltage between both ends of said capacitor from said command value of said virtual DC link voltage by a value obtained by subtracting said voltage between both ends from said rectified voltage.

7. The direct AC power converter according to any one of claims 1 to 6, further comprising

a second rectifying circuit that inputs said rectified voltage to said boost chopper.

8. The direct AC power converter according to any one of claims 1 to 6, wherein said pair of output terminals of said first rectifying circuit are connected to an

input side of said boost chopper.

9. The direct AC power converter according to claim 1 or any one of claims 3 to 8, wherein said discharge duty is always positive.

10. The direct AC power converter according to any one of claims 1 to 9, further comprising

a diode connected in parallel with said switch, a forward direction of said diode is a direction in which said capacitor is charged from said DC link.