

Fig. 1A

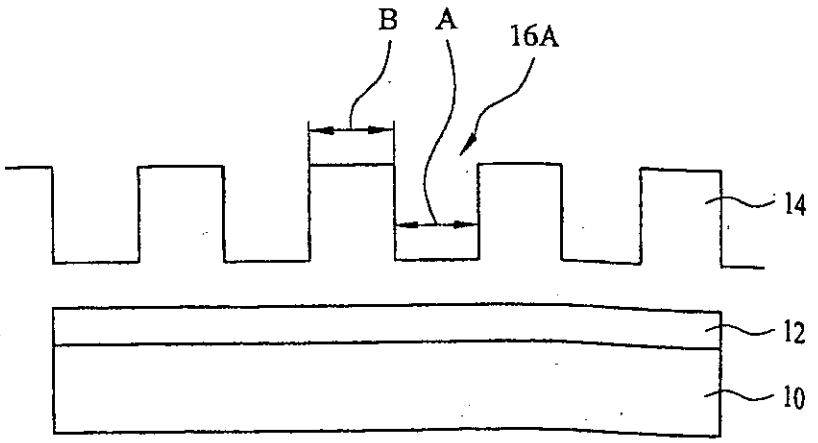


Fig. 1B

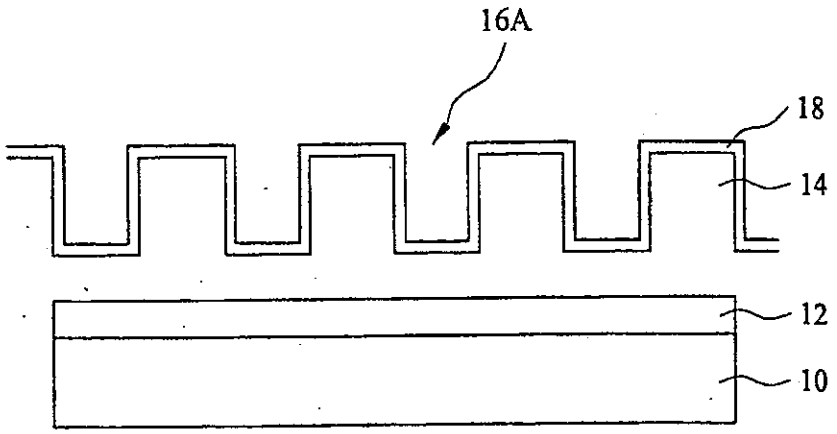


Fig. 1C

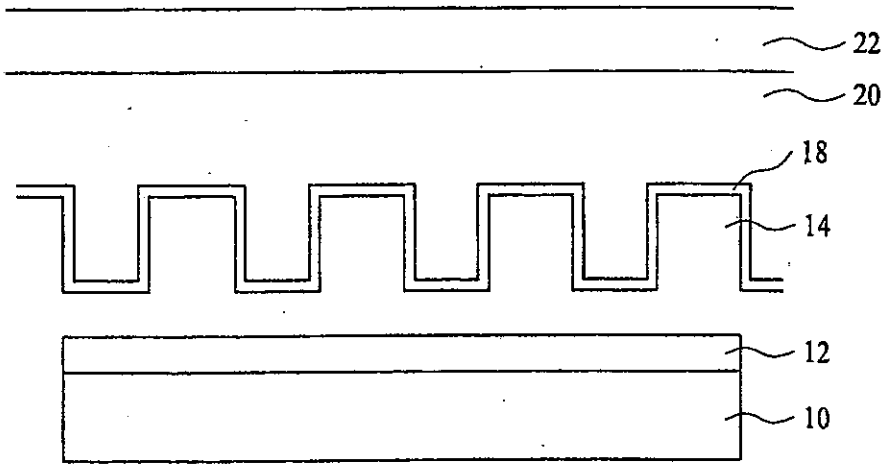


Fig. 1D

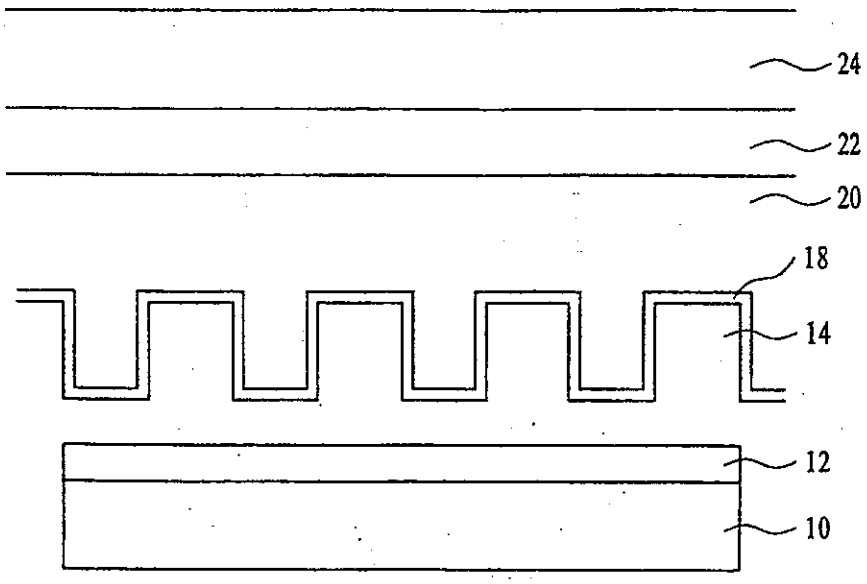

24
22
20
18
14
12
10

Fig. 1E

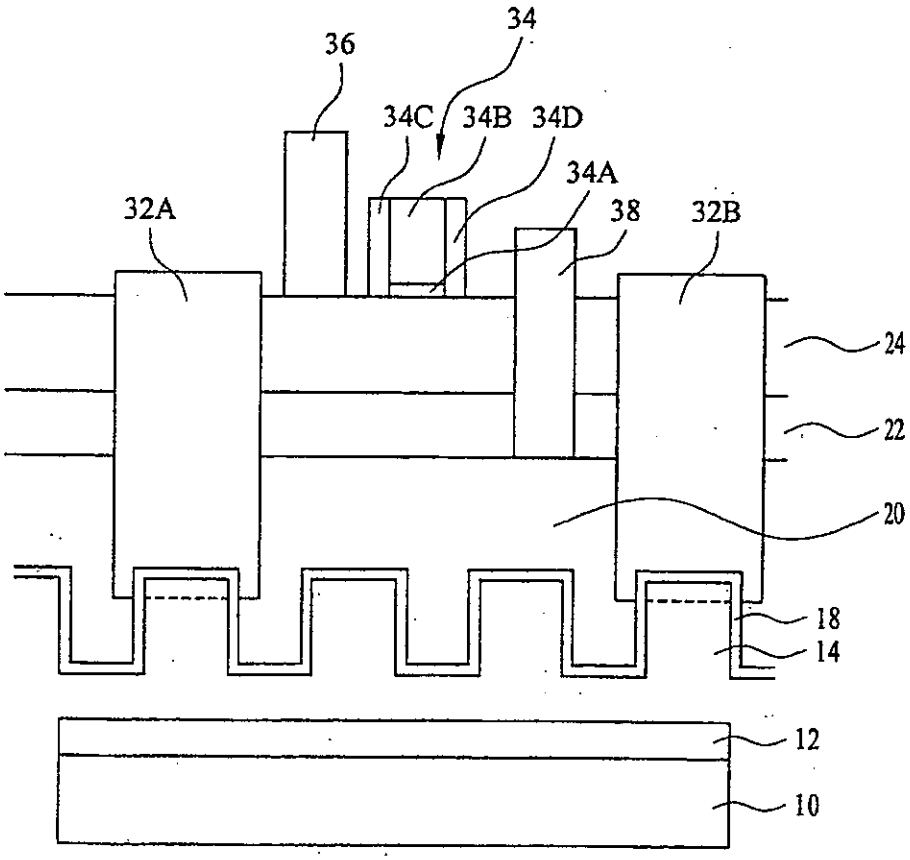

36
34
34C
34B
34D
34A
32A
38
32B
24
22
20
18
14
12
10

Fig. 2A

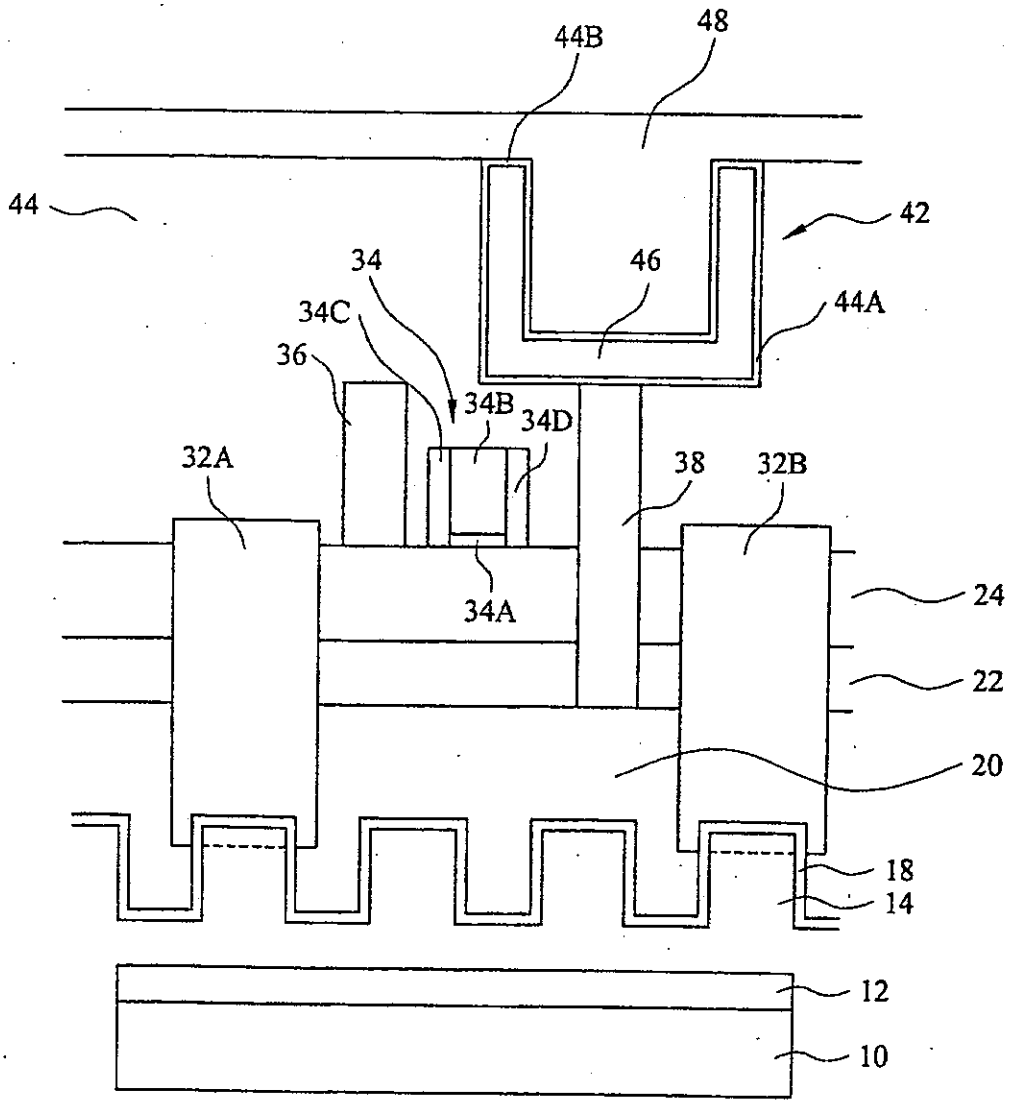

44B
48
44
42
34
46
34C
44A
36
34B
34D
32A
38
32B
34A
24
22
20
18
14
12
10

Fig. 2B

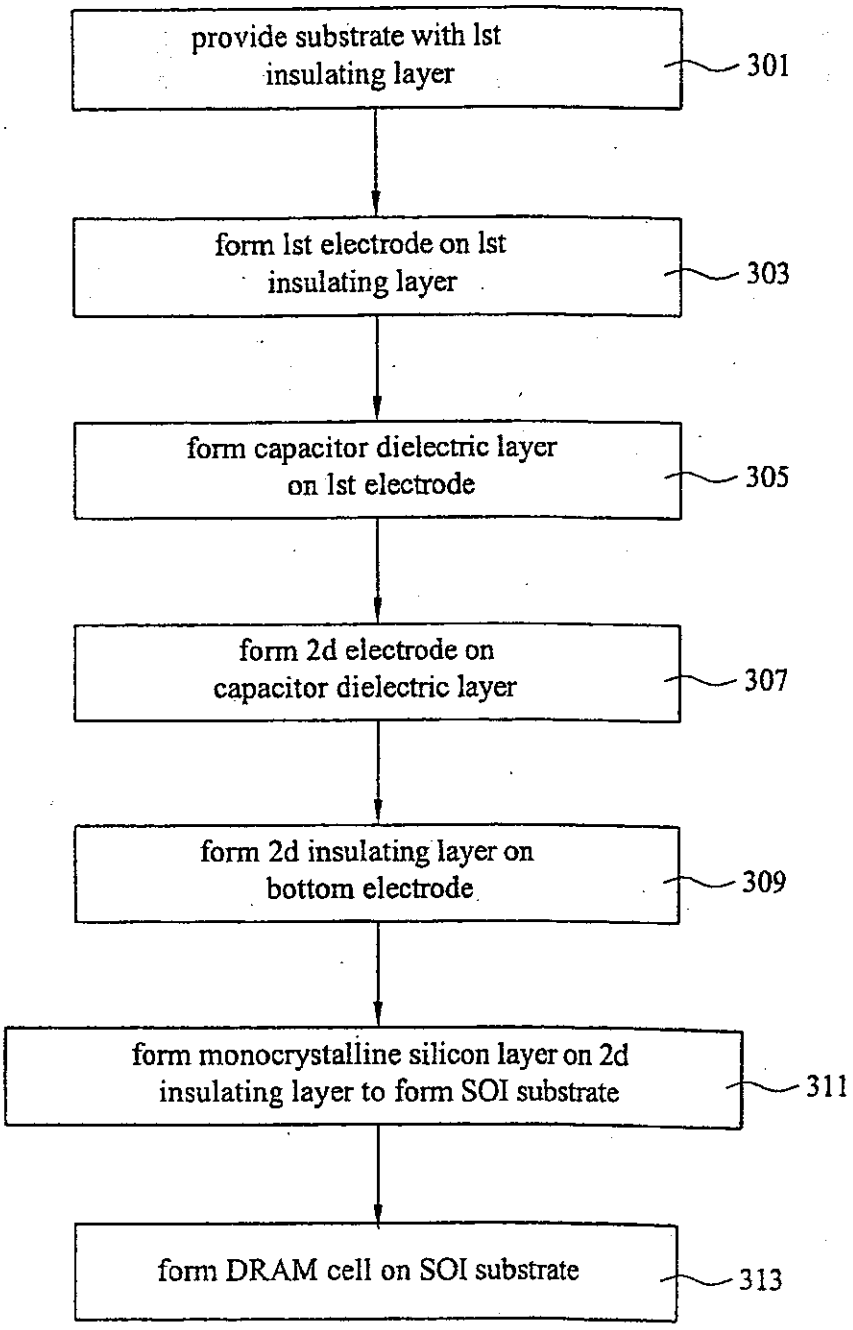

provide substrate with lst insulating layer
301
form lst electrode on lst insulating layer
303
form capacitor dielectric layer on lst electrode
305
form 2d electrode on capacitor dielectric layer
307
form 2d insulating layer on bottom electrode
309
form monocrystalline silicon layer on 2d insulating layer to form SOI substrate
311
form DRAM cell on SOI substrate
313

Fig. 3