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PROCESS FOR FABRICATING SEMICONDUCTOR DEVICE

ABSTRACT

A process for fabricating a semiconductor device comprising multilevel interconnection, comprising: forming a trench on the surface of a first substrate to provide an element isolating region; forming a first insulating film on the surface of the trench and the first substrate; forming a first interconnection layer on the surface of the first insulating film; forming a second insulating film on the surface of the first substrate in such a manner that the first interconnection layer is covered and the trench is filled; forming a second interconnection layer on the second insulating film; forming sequentially in this order, a third insulating film and an adhesion layer on the surface of said second insulating film covering the second interconnection layer; bonding a second substrate on the surface of the adhesion layer; planarizing the back of the first substrate by removing the first substrate from the back side thereof and the bottom of the trench; and forming a fourth insulating film on the back of the first substrate, and forming a third interconnection layer on the fourth insulating film. The process according to the present invention enables a semiconductor device comprising a multilevel interconnection with small step height.

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