ABSTRACT

METHOD TO FORM A SMOOTH GATE POLYSILICON SIDEWALL IN THE FABRICATION OF INTEGRATED CIRCUITS

A method for forming gate structures with smooth sidewalls by amorphizing the polysilicon along the gate boundaries is described. This method results in minimal gate depletion effects and improved critical dimension control in the gates of smaller devices. The method involves providing a gate silicon oxide layer on the surface of the semiconductor substrate. A gate electrode layer, such as polysilicon is deposited over the gate silicon oxide followed by a masking oxide layer deposited over the gate electrode layer. The masking oxide layer is patterned for the formation of the gate electrode. An ion implantation of silicon or germanium amorphizes the area of the polysilicon not protected by the masking oxide mask and also amorphizes the area along the boundaries of the polysilicon gate. Thereafter, the amorphized silicon is then removed by an anisotropic etch leaving a narrow area of amorphized silicon on the gate electrode sidewalls under the edges of the masking oxide mask completing the gate structure having smooth sidewalls.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)