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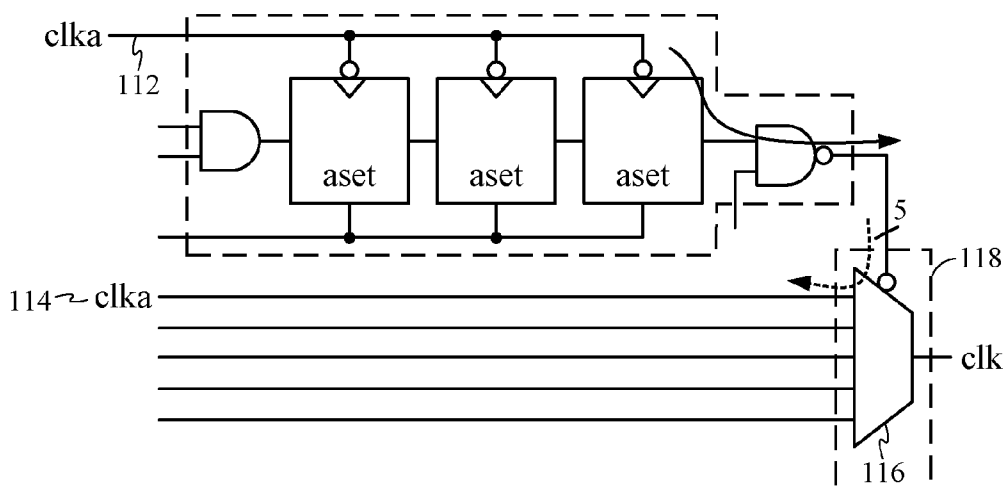
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(54) Title: A GLITCH-FREE CLOCK SIGNAL MULTIPLEXER CIRCUIT AND METHOD OF OPERATION THEREOF



(57) Abstract: Techniques for the design and use of a digital signal processor, including (but not limited to) for processing transmissions in a communications (e.g., CDMA) system. Reduced glitch occurs in switching from a first clock input to a second clock input driving a clock multiplexer. The clock multiplexer receives a first clock input and provides a clock output and determines a low phase output level in the clock output in response to a low phase input level in the first clock output. For a limited period of time, a low phase output level is forced irrespective of the phase level of the first clock input signal. The clock multiplexer receives a second clock input and determines a low phase input level in the second clock input signal. Switching to providing the clock output in response to the second clock input occurs during the low phase input level in the second clock input signal. Then, the output of the clock multiplexer follows the phase level of the second clock signal.

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