example, on any suitable surface, for example, one or more of the surfaces illustrated in FIG. 11. FIG. 11 illustrates a portion of a system in which a fluid surface 910 is contacted by a moving fluid during the production of a semiconductor product from the system and/or during monitoring of the system. In one embodiment, the fluid surface 910 is the interior of a flexible or rigid tube or pipe 911, through which a fluid such as gas and/or liquid flow(s), as indicated by arrows 912, or any other part in contact with the fluid and in fluid motion. FIG. 11 also illustrates an outer surface 913, which has a different composition or the same as the fluid surface 910.

[0068] In one embodiment, the coating 101, the layer 102, the functionalized layer 110, and/or the oxidized-then-functionalized layer 109 include(s) resistance to erosion (for example, from both solids and liquids) and corrosion. Resistance to erosion occurs in spite of an impinging particle or stream contacting the surface. Resistance to corrosion occurs by preventing surfaces from reacting with the environment and/or reaction products being formed as surface asperities. Such resistance prevents attrition of the reaction products from occurring as a result of crack formation and/or abrasion in the contact interactions of the materials.

[0069] The following Examples show various elements relating to the disclosure. Properties and parameters disclosed within the Examples should be considered as being disclosed within the Detailed Description of the Invention, whether comparative in nature or illustrative in nature.

EXAMPLE 1

[0070] A first example includes introducing dimethylsilane to the substrate 100 for 2 hours at 8 psia gas at 450°C to form the layer 102. The layer 102 is almost undetectable (i.e., very difficult to visually discern) on a mirror-polished 316 stainless steel coupon (slightly yellowed). Measurements show water contact angle data prior to the deposition treatment at around 60°. After the deposition treatment with dimethylsilane, the contact angle increases to around 102°. Although the layer 102 is not visible, the data indicates an extremely thin deposition with a significant density of carbosilyl material on the layer 102 of the surface 105. The thickness of the layer 102 is estimated to be at about 100 Angstroms, as available spectroscopic techniques are not sensitive enough to detect the

What is claimed is:

1. A semiconductor fabrication process, comprising:

providing a coated article, the coated article having a substrate and a layer applied to the substrate by decomposition and then oxidization of dimethylsilane through chemical vapor deposition, the layer applied by a fluid material; and then

positioning the coated article in a system for producing a semiconductor product.

2. The process of claim 1, wherein the layer includes oxidized dimethylsilane.

3. The process of claim 1, wherein the layer is applied to an oxidized layer, a pretreated layer, or a combination thereof.

4. The process of claim 3, wherein the oxidized layer includes an oxidized carbosilane material.

5. The process of claim 3, wherein the oxidized layer includes oxidized dimethylsilane.

6. The process of claim 5, wherein the layer includes trimethylsilane applied to the oxidized dimethylsilane.

7. The process of claim 1, wherein the fluid material is a gas.

8. The process of claim 1, wherein the fluid material is a plasma.

9. The process of claim 1, wherein the coated article is a tube and the layer is an internal surface of the tube, the coated article is a fitting and the layer is an internal surface of the fitting, the coated article is a pipe and the layer is an internal surface of the pipe, or the coated article is a chamber and the layer is an internal surface of the chamber wall.

10. The process of claim 1, wherein the semiconductor product comprises a crystalline solid, a poly-crystalline material, or an amorphous material.

11. The process of claim 1, wherein the semiconductor product includes an intrinsic semiconductor.

12. The process of claim 1, wherein the semiconductor product includes an extrinsic semiconductor having a positive charge conductor.

13. The process of claim 1, wherein the semiconductor product is selected from the group consisting of a pure element semiconductor and a compound semiconductor.

14. The process of claim 1, wherein the semiconductor product includes a surface consisting of indium antimonide (InSb), indium arsenide (InAs), indium phosphide (InP), gallium phosphide (GaP), gallium antimonide (GaSb), gallium arsenide (GaAs), silicon carbide (SiC), gallium nitride (GaN), silicon germanium (SiGe), or selenium sulfide (SeS).