CLAIMS

1. A semiconductor device, comprising: a substrate; a gate region on the substrate; a contact region on the substrate, wherein the contact region comprises a first portion and a second portion, wherein the first portion is in contact with the substrate and has a first top surface above the substrate and a first bottom surface on the substrate, wherein the first top surface is in contact with a dielectric layer, wherein the second portion is in contact with the substrate and has a second top surface above the substrate and a second bottom surface on the substrate, wherein the first portion is in contact with the second portion, wherein the first top surface has a first height above the substrate and the second top surface has a second height above the substrate, wherein the first height is smaller than the second height, and wherein the first bottom surface and the second bottom surface are coplanar with a bottom surface of the gate region; and a via on the second top surface of the second portion of the contact region.

2. The semiconductor device of claim 1, wherein the first height is around 30% to 50% of the second height.

3. The semiconductor device of claim 1, wherein the dielectric layer comprises Silicon Dioxide (SiO2).

4. The semiconductor device of claim 1, wherein the via comprises at least one of Copper (Cu), Tungsten (W), Ruthenium (Ru), and Cobalt (Co).

5. The semiconductor device of claim 1, wherein the gate region comprises a gate oxide layer, gate spacers, a metal gate, a cap layer, and a top dielectric layer.

6. The semiconductor device of claim 1, wherein the contact region comprises W.

7. The semiconductor device of claim 1, wherein the second top surface is coplanar with a top surface of the gate region.

8. A method for fabricating a semiconductor device, comprising: forming a plurality of gate regions on a substrate; forming a plurality of contact regions on the substrate, wherein each contact region of the plurality of contact regions comprises a first portion and a second portion,

wherein the first portion is in contact with the substrate and has a first top surface above the substrate and a first bottom surface on the substrate, wherein the first top surface is in contact with a dielectric layer, wherein the second portion is in contact with the substrate and has a second top surface above the substrate and a second bottom surface on the substrate, wherein the first portion is in contact with the second portion, wherein the first top surface has a first height above the substrate and the second top surface has a second height above the substrate, wherein the first height is smaller than the second height, and wherein the first bottom surface and the second bottom surface are coplanar with a bottom surface of a gate region in the plurality of gate regions; and forming a via on the second top surface of the second portion of each contact region.

9. The method of claim 8, wherein the first height is around 30% to 50% of the second height.

10. The method of claim 8, wherein the second top surface is coplanar with a top surface of the gate region in the plurality of gate regions.

11. The method of claim 8, wherein the forming the plurality of contact regions on the substrate comprises recessing the plurality of contact regions using dry etching.

12. The method of claim 8, wherein the dielectric layer comprises Silicon Dioxide (SiO2).

13. The method of claim 8, wherein the via comprises at least one of Copper (Cu), Tungsten (W), Ruthenium (Ru), and Cobalt (Co).

14. The method of claim 8, wherein the plurality of contact regions comprises W.