SINGLE AND DUAL STAGE WAFER CUSHION

FIELD OF INVENTION

This invention relates to improvements in a cushioning device for cushioning a stack of semiconductor wafers within a wafer transportation container. More particularly, the present cushioning device is a formed or folded ring with compound bends and surfaces that provide variable amounts of cushioning as the compound bends and surfaces engage.

DESCRIPTION OF RELATED ART

When semiconductor wafers are placed within a transportation container the stack of wafers are either loose or are compressed against the opposing houses. In either case, transportation of the semiconductor wafers can cause abrasion to some or all of the stacked wafers. Some patents have been filed using separator sheets, pads or foam rings to cushion the outer semiconductor wafers and absorb shock and movement as the semiconductor wafers are being transported.

Limiting radial movement becomes an important issue when shipping to prevent abrasion of the prime wafer surface, which may or may not contain circuitry. This is also true for bumped wafers that may or may not be stacked on spacer rings where the rings must only touch the periphery of the wafer and not shift radially into the areas containing the solder bumps. The Wafer Cushioning Rings ability to protect semiconductor wafers is enhanced when using a wafer container that reduces radial wafer shift.

If a rigid spacer is used the spacer can cause harm to the wafers and may not provide sufficient grip on the wafers to prevent movement. If a foam spacer is used the foam spacers are susceptible to damage and aging. Several products and patents have been filed that disclose these features. Exemplary examples of patents covering these products are disclosed herein.

U.S. Patent Number 3,392,824 issued July 16 1968 to S. F. Flynn and US Patent Number 5,366,079 issued October 22, 1994 to Chih-Ching Lin et al., both disclose packaging system for cushioning circuit wafer where the cushioning system is a Bellville type platter or a platter with flexed legs that extend from the center of the platter. While these patents disclose a cushioning system for wafers the cushions

slide radially on the outer surface of the wafers as the spacers are crushed within the transportation housing. This can cause damage to the wafers.

U.S. Patent Number 6,926,150 issued August 9, 2005 to Gonzlo Amador et al., and US Patent Number 7,530,462 issued May 12, 2009 to Toshitsugu Yajima et al., both disclose a wafer cushion using a rigid disk space. These patents are more related to spacers between the semiconductor wafers rather that providing cushioning and gap filling. In a number of cases these spacers are supplemented with foam pads located either across the entire surface of the wafer or on just the outer edges of the wafer.

U.S. Patent Number 7,425,362 issued September 16, 2008 to James R. Thomas et al and U.S. Patent Number 7,611,766 issued to Masahiko Fuyumuro on November 3, 2009 discloses a wavy pad where the high and low parts of the pad fill the space between the wafers and the transportation housing. These pads are made from a variety of materials from plastic to paper and are fabricated in variable profiles to accommodate the space between the wafers and transportation housing.

U.S. Patent Number 6,926,150 issued August 9, 2005 to Gonzalo Amador et al., U.S. Patent Number 7,316,312 issued January 8, 2008 to Pei-Liang Chiu and U.S. Patent Application Number 2002/0144927 to Ray G. Brooks et al that published on October 10, 2002 discloses a foam pad or ring to cushion the wafers within the packaging. The amount of force that is applied by a foam pad can be a significant variable as the foam ages. Foams can also be a cause of contamination as the foam cell structure breaks down. Foam particles can also be a contaminant that interferes with the doping of semiconductor wafers. In some cases the foam makes contact with the entire surface of the wafers and can cause deformation of the wafer(s).

What is needed is a cushioning ring that has a variable amount of cushioning to accommodate the minor variation on the top and bottom of a stack of semiconductor wafers. The pending design provides this solution with a single and dual stage wafer cushion.

BRIEF SUMMARY OF THE INVENTION

It is an object of the single and dual stage wafer cushion to operate with a wafer carrier where the cushion can be placed on both the bottom of the wafer carrier and on the top of wafers that are placed within the carrier. The cushion expands and collapses to accommodate variations in wafer thicknesses and variation in carrier housings. While the variation in wafer thickness on an individual wafer may be small, when the variations are accumulated the gap can be larger than desired. The cushioning provides minimal forces on the wafers and the housing to make the housing easy to open and further limit movement of the wafers within the wafer carrier.

It is an object of the single and dual stage wafer cushion to be manufactured to fit within the housing of a wafer carrier. The shape of the cushion is a folded ring where the fold is open on the outside diameter. The outside edge of the ring provides the greatest expansion such that only the outer edge of the ring makes contact with the outer edge of the wafer. This minimizes the contact area with wafer and places any axial load on the outer edge surface of the wafer where a wafer typically is placed on a separator disk to minimize damage to the inner surface of the wafers and minimize flexing of the center of the wafer(s).

It is another object of the single and dual stage wafer cushion to be made of a material where it can flex and absorb any shocks before the shock is transferred to the wafer stack. The material can be molded, thermoformed, cast or vulcanized.

It is another object of the single and dual stage wafer cushion to be made with a cross section shape having only half a "V" where the ring would be attached by bonding or clipping to the top and or bottom cover such that the cover provides the limiting function of the missing half of the "V". This design would be capable of having a single or dual stage version. This design allows single or multiple arms or "V rings" to be stacked to take up excess space inside the box.

It is another object of the single and dual stage wafer cushion to be made from a non-absorbent material. This prevents debris or contaminants from embedding into the wafer cushion and also prevent sheading of material from the wafer cushion.

It is still another object of the single and dual stage wafer cushion to use both an edge hinge as a single first stage hinge and a second mid span hinge for the dual

stage wafer. This dual stage design gives two distinctly different cushioning forces as opposed to using a single stage design where the force is liner with the amount of compression that is being applied to the outer surfaces of the wafer cushion.

Various objects, features, aspects, and advantages of the present invention will become more apparent from the following detailed description of preferred embodiments of the invention, along with the accompanying drawings in which like numerals represent like components.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 shows an isometric view of a single and dual stage wafer cushion.

FIG. 2 shows an isometric sectional view of the single and dual stage wafer cushion.

FIG. 3 shows an isometric sectional view of the single and dual stage wafer cushion in a second preferred embodiment.

FIG. 4 shows an isometric sectional view of the single and dual stage wafer cushion in a third preferred embodiment.

FIG. 5 shows an isometric view of the single and dual stage wafer cushion on a stack of semiconductor wafers without the top housing of the wafer shipper installed.

FIG. 6 shows an isometric view of the single and dual stage wafer cushion on a stack of semiconductor wafers with the top housing of the wafer shipper installed.

FIG. 7 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion in an uncompressed condition.

FIG. 8 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion initially compressed.

FIG. 9 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion partially compressed.

FIG. 10 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion more fully compressed.

FIG. 11 shows an isometric sectional view of the single and dual stage wafer cushion in a fourth preferred embodiment.

FIG. 12 shows an isometric view of the single and dual stage wafer cushion from the fourth preferred embodiment bonded to the bottom housing without wafers installed upon the wafer cushion.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows an isometric view of a single and dual stage wafer cushion 20 and FIG. 2 shows an isometric sectional view of the single and dual stage wafer cushion. The single and dual stage wafer cushion 20 from figure 1 shows essentially a ring shaped cushion where the inside of the wafer cushion 20 is open. In the preferred embodiment two single and dual stage wafer cushions 20 are placed on a stack of semiconductor wafers 40 as shown in figure 2. The stack of semiconductor wafers in this figure include spacer rings 50 is placed between each semiconductor wafer 40. The spacers 50 allow for stacking of "Bumped" wafers substrates with tiny solder balls used for electrical interconnection to the final product or external circuitry. Bumped wafer stacks are normally used with solid height, non-adjustable spacer rings 50 between the wafers to prevent the solder balls (bumps) from being damaged by contact with adjacent substrates 40.

This first preferred embodiment is a ring designed with a dual spring rate or variable spring rate. The dual stage version 20 has one spring rate for easy loading and closing of the shipper top cover (not shown), whereas the second stage of the spring provides a stiffer spring rate to absorb energy if the shipper is dropped or mishandled, thus protecting the wafer stack or substrate stack.

With the cushion configured as a "V Ring" the cross section is shaped like a "V" to provide a spring or cushioning for the wafers. This design lends itself to the injection molding process, vulcanization or other manufacturing methods with the V shaped cross section. The tip 23 of the V provides the point of contact to the wafer and the shipping container. There is also a case where multiple stacking "V rings" can be used to take up excess space inside the wafer shipping container. One advantage of the "V" shape is that it allows the ring to only contact a small zone 23 and 34 on the wafer 40 near the perimeter. For bumped wafers, there is normally a 3 mm wide exclusion zone for circuitry or solder bumps that extends inward from the perimeter of the wafer. Our preferred embodiment has a slightly raised zone with radius at the point of wafer contact, but it does not have to have this feature. The

slightly raised area at the tip of the "V" allows additional clearance for any solder bumps that are near the "keep out" zone. Figure 2 shows a two separate wafer cushions with a lower cushion placed into the wafer carrier 21 under all of the wafers 40. The outside diameter edge 23 of the lower cushion is sized to fit within the wafer carrier 21 with the lower bottom surface 22 supported on the bottom of the wafer carrier 21 support.

The weight of the wafers 40 and support rings 50 at least partially load the lower wafer cushion whereby at least partially compressing the lower cushion such that the first stage or inside diameter 30 hinge 31 of the wafer cushion at least partially compress the wafer cushion. It should be noted from figure 2 that when the first stage is compressed a second cushion gap is still visible both inside and outside of the middle surface 32. Figure 2 further shows that when the first stage has made contact only the outer diameter edge 34 makes contact with the outer edge of the semiconductor wafer 40 and the remaining inner diameter surfaces of the wafer cushion "float" above the semiconductor wafer without making contact with the surface of the semiconductor wafer(s). When the top housing (not shown) of the wafer carrier is installed the top housing compresses the top surface 35 of the upper wafer cushion and loads the lower wafer cushion whereby providing even cushion between the top and the bottom wafer cushion.

FIG. 3 shows an isometric sectional view of the single and dual stage wafer cushion in a second preferred embodiment. In this embodiment the wafer cushion 20 has an inner lip 60 that provides additional strength for the hinge 65 and also provides a gripping surface for easier removal of the wafer cushion 20. The outside diameter 64 is sufficiently sized to center the wafer cushion within a wafer carrier. The top 61 and bottom surface 62 of the wafer cushion 20 has a slight radial curve to maintain contact with just the outer edge top or bottom surface of a semiconductor wafer. It is further contemplated that a portion 66 of the cushion can be broken, serrated or formed to create multiple finger portions that independently flex from the inside diameter hinge 65. In the embodiment shown the void areas 66 exists through both the upper and lower lips or arms but could also be formed to exist only through one leg of the cushion whereby leaving the other leg continuous. At the first stage of compression the inside outer surfaces 64 of the wafer cushion come in contact and

leave an air gap from the inside hinge area 65 to the outer surfaces to provide the second stage of cushioning.

FIG. 4 shows an isometric sectional view of the single and dual stage wafer cushion 20 in a third preferred embodiment. This third preferred embodiment will be briefly described in this figure and described in more detail in figures 5 to 10. This embodiment has a plurality of flexible arms that extend from the inside diameter hinge area 70 and 75. The extreme upper and lower surfaces 71 make contact with the outer upper and lower surfaces of a semiconductor wafer when the wafer cushion is installed in a wafer carrier. The extreme outer diameters(s) 73 are sufficiently sized to fit within a wafer carrier and provide little or no movement within the wafer carrier. The wafer cushion is shown in an expanded and in a first stage compressed stage in figures 5 and 6 within a wafer carrier.

FIG. 5 shows an isometric view of the single and dual stage wafer cushion on a stack of semiconductor wafers without the top housing of the wafer shipper installed and FIG. 6 shows an isometric view of the single and dual stage wafer cushion on a stack of semiconductor wafers with the top housing of the wafer shipper installed. From Figure 5 and 6 the lower cushion is compressed with the lower lip 22 in contact with the bottom housing 21 and the upper lip 23 in contact with the lowest semiconductor wafer 40. The stack of semiconductor wafers 40 are each separated with a wafer separator 50 placed between each semiconductor wafer 40. In figure 5 the upper wafer cushion is shown uncompressed where the first or single stage of cushion is not compressed and the middle of the extended arms are not in contact at mid span 76 and 77. The bottom surface of the wafer cushion at 72 is in contact with the outer top surface of the top semiconductor wafer 40. The tangent arched top surface of the wafer cushion 71 provides generally just a linear point contact with the semiconductor wafer 40 and the top 25 or bottom 21 housing. The outer edge 74 and 78 of the cushion approximates the outside diameter of the semiconductor wafers 40.

When the top housing 25 is lowered onto the wafer cushion the arms will move closer together as they hinge from the inner radius 70. When the housings 21 and 25 are secured the top housing will push upon the outer edge 26 of the top wafer cushion and the central portion 77 of the arms will make contact and form the first stage of cushion.

FIG. 7 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion in an uncompressed condition, FIG. 8 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion initially compressed, FIG. 9 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion partially compressed and FIG. 10 shows a side sectional view of the single and dual stage wafer cushion with the wafer cushion more fully compressed. Starting with figure 7 the wafer cushion 20 is in a natural uncompressed condition without any forces 100 and 101 causing the cushion to compress. The hinge 70 and 75 creates a curve to keep the arms on an open "U" or "V" configuration. The top 71 and bottom surfaces 72 of the wafer cushion are at the greatest dimension. The outer lip 74 and 78 are essentially the same dimension, but it is contemplated that they can exist at different radii as well. The central 76 and 77 or second (dual) stage of the arms open and not in contact.

In figure 8 forces 100 and 101 cause the arms to compress and the interior area begins to compress. Both the end 70, 73 and the mid-section elbow, profile or hinges 76 and 77 flex as the force increases until the inner surfaces of the arms make contact as shown in figure 9. The force 100 and 101 creates a first load or spring constant profile.

At this stage the resisting spring force to provide a cushion changes because the length of the lever arms has been shortened. In the embodiment shown the contact between the arm segments is approximately at mid span, but it is contemplated that the central contact can take place at any point in the span of the arms to yield a different cushion force profile. The profile shown in figure 9 represents the condition where the housings are closed and in a normal shipping mode. Additional applied force between the forces shown in figures 9 and 10 100/101 verses 102/103 provides a second load or spring constant that is different from the load or spring constant as applied from figures 7 to 9. The spring constant can be linear stepped or non-linear based upon the shape, angles and constant or variable thicknesses of the hinge and or leg section(s).

Figure 10 shows a shock load condition that might occur when the wafer carrier is dropped or bumped. The forces 102 and 103 continue to push on the extreme ends of the arms. The outer lengths of the arms are in compression along their

length(s). It should be noted that even at this loading an air gap 79 still provides some further cushioning and the inside on the cushion still provides a space for clearance of components that may be placed on the semiconductor wafers.

FIG. 11 shows an isometric sectional view of the single and dual stage wafer cushion 29 in a fourth preferred embodiment and FIG. 12 shows an isometric view of the single and dual stage wafer cushion from the fourth preferred embodiment bonded to the bottom housing without wafers installed upon the wafer cushion.

"Single Sided Ring"- One version of the cushioning ring 29 described above is a ring with a cross section shape having only half a "V" where the ring would be attached, (bonded or clipped) to the top or bottom cover such that the cover provides the limiting function of the missing half of the "V". This design would be capable of having a single or dual stage version. This design allows multiple "V rings" to be stacked to take up excess space inside the box. The bottom of this cushion 90 can be bonded to the lower housing 21 (or 25). While this single sided ring has only one arm the arm has a similar configuration with an inside hinge area 91 and 92, a mid-span elbow 93 to form a division between the first and second stage of the cushion. The outer edge 95 is sized to provide clearance of the housing 21 wall to provide free movement and flexing. The top edge of the wafer cushion 96 is configured to make contact with just the outer edge of the wafer separator or the semiconductor wafer (not shown). The lower radii 94 provide additional shock cushioning when the wafer stack flattens the majority of the wafer cushion 29.

In the preferred embodiment the wafer cushion is made from a compliant material having a hardness of shore D of between 10 and 70 but other hardness are contemplated based upon the material that is being cushioned and the stack height / weight that is being cushioned. It is also contemplated that the upper and lower wafer cushions being used in a wafer shipper can have different properties and configurations based upon the weight or the fact that the semiconductor wafers exist above or below the wafer cushions. The profile from the central hinge to the outer contact points can be curved, or have variable cross section, or multiple steps, profiles, elbows or bends to achieve non-linear cushion forces or multiple stage wafer cushions.

Thus, specific embodiments of a single and dual stage wafer cushion have been disclosed. It should be apparent, however, to those skilled in the art that many more modifications besides those described are possible without departing from the inventive concepts herein. The inventive subject matter, therefore, is not to be restricted except in the spirit of the appended claims.

CLAIMS

1. A single stage wafer cushion comprising :

a cushion having a continuous ring shape;

the ring shape consisting of a "V" or "U" cross section wherein an opening of the "V" or "U" is opened on the outer peripheral end of the ring;

the ring being made of a compliant material with a hinging portion formed at an inner diameter;

an upper and a lower contact surface located on a top edge and a bottom edge of the opened outer peripheral end such that,

when force is applied to the upper and lower contact surface the hinge portion will flex to close the opened outer peripheral end;

wherein the cushion is a single unit.

2. The single stage wafer cushion according to Claim 1 wherein the upper contact surface is configured to rest on a housing of a wafer carrier.

3. The single stage wafer cushion according to Claim 1 wherein the lower contact surface is configured to rest on a semiconductor wafer.

4. The single stage wafer cushion according to Claim 1 wherein when force is applied to the top and the bottom edge of the opened outer peripheral end a cushion is created having a linear spring constant.

5. The single stage wafer cushion according to Claim 1 wherein when force is applied to the top and the bottom edge of the opened outer peripheral end a cushion is created having a non-linear spring constant.

6. The single stage wafer cushion according to Claim 1 wherein at least one peripheral end of the ring is serrated.

7. The single stage wafer cushion according to Claim 1 wherein when the top and the bottom edges of the opened outer peripheral end come in contact with each other, an outside diameter thickness is created that is greater than a thickness of the inside diameter.

8. A single and dual stage wafer cushion comprising :

a compliant continuous ring having an inner diameter and an outer diameter;

the ring shape consisting of a single “V” or “U” cross section wherein an opening of the “V” or “U” is opened on the outer peripheral end of the ring;

the inner diameter having a hinge profile with a first leg extending from the hinge profile to the outer diameter and the first leg having an inner and an outer top surface;

a second leg extending from the hinge profile to the outer diameter and having an inner and an outer bottom surface to form an opening between the first leg and the second leg at the outer diameter, and

the first leg and the second leg are spaced from the inner diameter;

wherein the cushion is a single unit.

9. The single and dual stage wafer cushion according to Claim 8 wherein the first and the second leg further include an elbow section between the hinge profile and the outer diameter.

10. The single and dual stage wafer cushion according to Claim 9 wherein the elbow sections bend towards each other.

11. The single and dual stage wafer cushion according to Claim 10 wherein, when force is applied to the outer top surface and the outer bottom surface, the first leg and the second leg are brought together allowing the elbow sections to make contact whereby providing a first stage cushion.

12. The single and dual stage wafer cushion according to Claim 11 wherein, when additional force is applied to the outer top surface and the outer bottom surface, the first leg and the second leg of the wafer cushion will provide a second dual stage cushion where a spring constant of the first stage is different from a spring constant of the second stage.

13. The single and dual stage wafer cushion according to Claim 8 wherein the outer bottom surface is configured to rest on a housing of a wafer carrier.

14. The single and dual stage wafer cushion according to Claim 8 wherein the outer top surface is configured to rest on a semiconductor wafer.

15. A single and dual stage wafer cushion comprising :

a compliant continuous ring having an inner diameter and an outer diameter;

the ring shape consisting of a single "V" or "U" cross section wherein an opening of the "V" or "U" is opened on the outer peripheral end of the ring;

the ring having a first bottom surface and a first top surface;

the bottom surface having an essentially planar surface at the inner diameter;

at least one elevation change from the essentially planar surface at the inner diameter to a second bottom surface,

whereby the at least one elevation change provides a cushion having a first spring constant when a load is applied between the first bottom surface and the first top surface;

wherein the cushion is a single unit.

16. The single and dual stage wafer cushion according to Claim 15 that further includes a bent profile located between the essentially planar surface and the inner diameter to a second bottom surface.

17. The single and dual stage wafer cushion according to Claim 16 wherein the bent profile provides a second spring constant when compliant ring is compressed to the bend profile.

18. The single and dual stage wafer cushion according to Claim 15 wherein the first bottom surface is configured to rest on a housing of a wafer carrier.

19. The single and dual stage wafer cushion according to Claim 18 wherein the first bottom surface is bonded to the housing of the wafer carrier.

20. The single and dual stage wafer cushion according to Claim 15 wherein the first top surface is configured to rest on a semiconductor wafer.