

cylinders. In some embodiments, the conductive pillar 120, electrode cylinder 130, and memory material 115 may be formed as other concentric shapes. The memory material 115 may include a chalcogenide. In some embodiments, the chalcogenide material may be a phase change material. In some embodiments, the memory material 115 may include a ternary composition that may include selenium (Se), arsenic (As), and germanium (Ge). In some embodiments, the memory material 115 may include a quaternary composition that may include tellurium (Te), Se, As, and Ge. Other materials may also be used. In some embodiments, the memory material 115 may be selectively deposited in the same plane as the electrode plane 110 to form memory cell 140. This alternative embodiment is shown in Figure 1 as memory column 180. As shown with memory column 180, the memory material 115 may not extend the entire length of the column 150.

[022] Figures 2A-C are illustrations of the portion of the 3D memory array 100 shown in Figure 1. Figure 2A is a top-down view of the portion of the 3D memory array 100. While Figure 2A illustrates one electrode plane 110, it will be appreciated that the memory array 100 may include additional electrode planes 110. With reference to Figure 2A, the memory columns 150 extend into the page as viewed by a reader. The memory columns 150 extending through the 3D memory array 100 may be seen in Figures 1, 2B, and 2C. Ring shaped memory cells 140 (Shown in Figures 2B and 2C) are aligned in the electrode plane 110, resulting from the memory columns 150 (Figure 1) formed in the openings 155 in the stack of electrode planes 110 and dielectric material. As previously discussed, the memory cells 140 are formed from the memory material 115 and may be ring-shaped in the plane of the electrode plane 110. Although shown as a ring-shape in the embodiment illustrated in Figure 1 and 2A-C, the memory material 115 may be formed as other shapes (e.g., rectangle, oval, irregular).

[023] The memory material 115 may be coupled to the one or more electrode planes 110 to form the memory cells 140. The memory material 115 may be further coupled to a conductive pillar 120. The conductive pillar 120 may extend through the stack of electrode planes and dielectric material. That is, it would extend into the page as viewed by a reader. The conductive pillar 120 extending through the stack may be seen in Figures 1, 2B, and 2C, where the conductive pillar 120 extends parallel to the plane of the page. Although shown as a cylinder-shape in the embodiment illustrated in

135. A conformal layer may be formed in the openings to form the memory material 115. The electrode cylinder 130 may be formed from a second conformal layer, and a conductive pillar 120 is formed to fill the remaining opening. In some embodiments, the electrode cylinder 130 may be omitted. Alternatively, the openings 155 may be filled with the memory material 115 then a second set of openings formed in the memory material 115. The second set of openings may be filled with the electrode cylinder 130 and a third set of openings formed in the electrode cylinder 130. The third set of openings may be filled to form the conductive pillars 120. A combination of forming openings and depositing conformal layers within the openings may also be used. The conductive pillars 120 and electrode planes 110 may then be coupled to memory access lines included in a memory array.

[029] In some embodiments, not shown in Figures 3A-C, recesses may be formed in each of the electrode planes 110 after openings 155 are formed. A conformal layer of memory material 115 may be selectively formed in the recesses. In some embodiments, this may selectively provide memory material 115 in the same plane as the electrode planes 110 without providing memory material 115 in the same plane as the dielectric material 135.

[030] The memory cell 140 may be written to store one of at least two different logic states (e.g., '1,' '0') by a write operation. In some embodiments, a memory material 115 may include multiple memory cells 140 and each of the memory cells 140 may be independently written to store one of the at least two logic states. In some embodiments, the different logic states may be defined by different threshold voltages (V_{TH}) of the memory cell 140. The threshold voltage exhibited by the memory cell 140 may be based on a polarity of a write pulse applied to the memory cell 140 during a write operation and on a polarity of a read pulse applied to the memory cell 140 during a read operation. The write pulse and read pulse may be applied to the memory cell 140 using the electrode plane 110 and conductive cylinder 120.

[031] The memory cell 140 may be configured as a two-terminal device between the electrode plane 110 and conductive cylinder 120 in some embodiments. A first logic state may be written to the memory cell 140 by applying a voltage (e.g., a write pulse) across the memory cell 140 in a first polarity. A second logic state may be written to the memory cell 140 by applying a voltage (e.g., a write pulse) across the memory cell

140 in a second polarity, which may be opposite to the first polarity. The memory cell 140 is read by applying a voltage (e.g., a read pulse) across the terminals. The memory cell 140 may always be read with the same polarity. For example, in some embodiments, the memory cell 140 is read by applying a voltage across the memory cell 140 in the first polarity. In other embodiments, the memory cell 140 is read by applying a voltage across the memory cell 140 in the second polarity. When the memory cell 140 is read with the same voltage polarity with which it was written, the memory cell 140 may exhibit a first V_{TH} . When the memory cell 140 is read with the opposite voltage polarity with which it was written, the memory cell 140 may exhibit a second V_{TH} . The different threshold voltages may be used to represent different logic states.

[032] When the memory cell 140 is a two-terminal device, the relative values of the voltages between the terminals determines the magnitude and polarity applied across the memory cell 140. For example, providing a voltage of 3V to the conductive cylinder 120 and 0V to the electrode plane 110 applies the same magnitude and polarity as providing a voltage of 6V to conductive cylinder 120 and 3V to electrode plane 110. As used herein, forward polarity indicates that the conductive cylinder 120 is set at a higher voltage than the electrode plane 110 and reverse polarity indicates that the conductive cylinder 120 is set at a lower voltage than the electrode plane 110. However, the use of “forward” and “reverse” polarities is by way of example, and the embodiments of the invention are not limited to those of the particular polarity direction described herein.

[033] Figure 4 is a voltage plot 400 of threshold voltages V_{TH1} , V_{TH0} for two logic states $State_1$, $State_0$ of a memory cell according to an embodiment of the disclosure. The threshold voltages of the memory cell are the threshold voltages observed when the memory cell is read. The memory cell may be read using a read voltage in the same polarity each time it is read, for example, in forward polarity. V_{TH1} may be observed in the memory cell when the memory cell was written to in the same polarity as the read voltage. For example, the memory cell may have been written to in a forward polarity and is then read in forward polarity. V_{TH1} may correspond to logic state $State_1$. Conversely, V_{TH0} may be observed in the memory cell when the memory cell was written to in the opposite polarity as the read voltage. For example, the memory cell may have

been written to in a reverse polarity and is then read in a forward polarity. V_{TH0} may correspond to logic state $State_0$. As illustrated by Figure 4, in some embodiments, different threshold voltages may be observed for the memory cell written and read in opposite polarities in comparison to the memory cell written and read in the same polarity.

[034] Figure 5 is a voltage plot 500 of two write pulses 505, 510 according to an embodiment of the disclosure. The write pulses 505, 510 may be used to write a logic state to a memory cell, such as memory cell 140 shown in Figures 1 and 2A-C, during a write operation. The write pulses may be applied by providing a first voltage to the conductive pillar and providing a second voltage to the electrode plane. The resulting voltage applied to the memory cell is the difference between the first and second voltages. The write pulses may be the same duration as read pulses. In some embodiments the duration is 10ns-50ns. In some embodiments, the duration is 1-100ns. Writing to the memory cell may take the same time as reading the memory cell in some embodiments.

[035] The polarity of the write pulses may be either a first polarity or a second polarity (e.g., forward or reverse). Write pulse 505 may apply a voltage V_{W1} to a memory cell in a first polarity (e.g., conductive cylinder at 6V and electrode plane at 0V). The polarity of the write pulse 505 may be the same as the polarity of read pulses. This may write a first logic state ($State_1$) to the memory cell. As shown in Figure 4, when write pulse 505 writes $State_1$ to the memory cell, the memory cell exhibits threshold voltage V_{TH1} when read.

[036] Write pulse 510 may apply a voltage V_{W0} to the memory cell in a second polarity (e.g., conductive cylinder at -6V and electrode plane at 0V). Write pulse 510 may have the opposite polarity of write pulse 405 and read pulses. Write pulse 510 may write a second logic state ($State_0$) to the memory cell. As shown in Figure 4, when write pulse 510 writes $State_0$ to the memory cell, the memory cell exhibits threshold voltage V_{TH0} when read.

[037] In some embodiments V_{W0} and V_{W1} may have the same voltage magnitude. In some embodiments, V_{W0} and V_{W1} may have different magnitudes. The magnitudes of V_{W0} and V_{W1} may be selected to be greater than or equal to the greater of threshold voltages V_{TH0} and V_{TH1} of $State_0$ and $State_1$, respectively. For example, $|V_{W0}| = |V_{W1}| = 6V$, $V_{TH1} = 4.5V$, and $V_{TH0} = 5.5V$. In some embodiments, the write pulses may have