

ABSTRACT

Provided is a multiply-accumulate operation apparatus capable of sufficiently restraining a sneak current even when it employs a precharge system in which the magnitude of an electric current flowing through an output line is detected. In a synapse operation section, multiple memory cells 17 each storing a synaptic connection weight therein are arranged in a matrix of rows and columns. Output lines MAL are each connected to the memory cells 17 in the corresponding column, and input lines DL1, DL2... are each connected to the memory cells 17 in the corresponding row. Each of the output lines MAL is precharged, and then its electric potential is decreased after the corresponding memory cells 17 discharge the output line MAL by allowing cell currents corresponding to their synaptic connection weights to flow therethrough. Each of the memory cells 17 is constituted of a memory element 21 in which a memory transistor MT, a drain side transistor DT, and a source side transistor ST are connected in series, and is connected between the corresponding one of the sets of the input lines DL1, DL2... and the output lines MAL. The memory transistor MT is configured to store a synaptic connection weight according to the amount of charge in a charge storage layer 24.