FIELD OF THE INVENTION

Embodiments of the present invention relate to semiconductor integrated circuits, and more particularly to field effect transistors, and methods for fabricating the transistors.

BACKGROUND

Quantum wells are formed in semiconductor devices such as diode lasers, High Electron Mobility Transistors (HEMTs) used in low-noise electronics and infrared photodetectors used for infrared imaging. Particularly, a quantum well is a potential well that confines particles, which were originally free to move in three dimensions, to two dimensions, forcing them to occupy a planar region. The effects of quantum confinement take place when the quantum well thickness becomes comparable at the de Broglie wavelength of the carriers (generally electrons and holes); leading to energy levels called "energy subbands", i.e., the carriers can only have discrete energy values.

Quantum wells are formed in semiconductors by having a material, like gallium arsenide sandwiched between two layers of a material with a wider bandgap, like aluminum arsenide. These structures can be grown by molecular beam epitaxy or chemical vapor deposition with control of the layer thickness down to monolayers.

In order to achieve high mobility quantum well device structures, a key element is the ability to confine dopants in close proximity to the intrinsic quantum well. Such a requirement is not easily met in many cases due to the uncontrolled diffusivity of such dopants. The dopants in a delta doped layer can diffuse or “spill into” the quantum well during the subsequent growth and annealing steps and hence degrade the device mobility/performance.

A partial solution to the problem of dopant out-diffusion from the delta doped layer during subsequent dopant activation annealing steps is the use of ultra fast ramping RTA (rapid thermal annealing). This does not address dopant diffusion/spread entirely though since dopants can also diffuse during the

formation, etc. may not be compatible with the ultra low thermal budget requirements for maintaining the delta doped layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

Figures 1 illustrates one embodiment of a method of fabricating a quantum well device;

Figures 2-6 illustrate one embodiment of various stages in the fabrication of a quantum well device; and

Figures 7A and **7B** are graphs illustrating dopant diffusion.

DETAILED DESCRIPTION

A mechanism for forming a doped quantum well structure is described. In the following detailed description of the present invention numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

As Complementary Metal-Oxide Semiconductor (CMOS) devices continue to scale down the gate length, one device parameter that is severely impacted by the continual increase of dopants in the channel is the carrier mobility. Thus, remotely doped quantum well structures are increasingly being implemented. The

surface roughness and impurity scattering (e.g., dopant not present in the quantum well) in the channel, and incorporation of strain in quantum well and with strain stabilization from bottom and cap hetero-epitaxial (Epi) layers. However, as discussed above, dopant out diffusion is a main concern of controlling the high concentration of dopants in the delta doped layer.

According to one embodiment, a quantum well structure is fabricated by forming of a diffusion barrier material on either side of a delta doping layer in order to confine the dopants in close proximity to a quantum well. In such an embodiment, a hetero-epitaxial quantum well structure is grown with a high mobility, narrow band gap, channel layer that is sandwiched between two wider bandgap layers. The electronic band structure at the hetero-junction interface confines either electron or hole carriers using conduction band offset or valence band offset, respectively.

During the growth of the wide band gap layers, heavily doped delta doping layers are grown sufficiently close to the quantum well layer as a carrier reservoir. Prior and after growth of the heavily doped delta layer, thin dopant diffusion barrier layers are grown above and below the heavily doped delta doping layer. The dopant diffusion barrier is formed, in one embodiment, by introducing a layer which has low dopant diffusivity (such as Si in a Ge quantum well structure), or by adding impurity in the wide band gap layers to suppress dopant diffusion (e.g. by adding carbon (C) in Si or SiGe to effectively suppress Boron (B) and Phosphorus (P) diffusion).

Figure 1 illustrates one embodiment of fabrication processes of one embodiment of a Ge quantum well and a sharp boundary delta doping layer. At processing block 110, a quantum well structure is formed by grading a transitional SiGe layer and a thick relaxed film Epi layer (e.g., Si1-xGex) to reduce dislocation defect of the Ge quantum well layer. **Figure 2** illustrates one embodiment of the graded SiGe and Si1-xGex layers formed on the Si substrate.

Referring back to **Figure 1**, a Si1-yGey layer is formed with the Ge composition tailored to have a desired valence band offset with the Ge quantum well valence band, processing block 120. **Figure 3** illustrates one embodiment of

Si1-yGey layer, processing block 130. **Figure 4** illustrates one embodiment of the formed Ge quantum well layer. Referring back to **Figure 1**, a Si barrier/heavily doped Si1-yGey/Si barrier sandwich is grown to contain the delta dopants, processing block 150. **Figure 5** illustrates one embodiment of the Si barrier/heavily doped Si1-yGey/Si barrier formed over the Ge quantum well layer.

Referring back to **Figure 1**, industry standard CMOS processing is then carried out to fabricate the remainder of the Ge QW PMOS device on the above substrate, processing block 150. Such processing includes**. Figure 5** illustrates one embodiment of a quantum well device having a diffusion layer surrounded delta doping area. In other embodiments, the diffusion barrier/delta doping layer stack can also be placed under the quantum well.

Figures 7A and **7B** illustrate examples of dopant diffusion barrier layers on blanket wafers for the case of high mobility Germanium (Ge) quantum well layers. The figures show mass spectrometry (SIMS) profile of Phosphorus in a Ge Epi layer grown on a silicon (Si) substrate. A thin 50A Si or a 50A 69% SiGe layer is embedded in Ge as a dopant diffusion layer. Comparing the 50A Si barrier in **Figure 7A** and the 50A 69% SiGe barrier of **Figure 7B**, the 50A Si effectively blocked the P diffusion in the top n-Ge from diffusing into the undoped i-Ge bottom layer.

Although described above with respect to a GE quantum well structure and, the above-described method may be implemented in other embodiments using any kind of high mobility quantum well structure. In further embodiments, any kind of diffusion barrier may be implemented; including a C doped Si or SiGe.

Figure 8 illustrates that quantum well devices 800, according to various embodiments of the invention, may be used in an integrated circuit 810 (or another chip, monolith device, semiconductor device, or microelectronic device, as they are generally understood in the field) and incorporated into a computer system 850 (or other electrical system). The computer system, which may be a portable, laptop, desktop, server, mainframe, or other computer system, may also include other conventional computer system components, such as a bus to communicate data, a memory to store data (e.g., main memory, read only memory, and/or a mass

electrical systems.

Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims, which in themselves recite only those features regarded as essential to the invention.

What is claimed is:

1. A method of fabricating a quantum well device comprising forming a diffusion barrier on sides of a delta layer of a quantum well to confine dopants to the quantum well.

2. The method of claim 1 further comprising forming the quantum well with a high mobility, narrow band gap channel layer.

3. The method of claim 1 wherein an electronic band structure at a hetero-junction interface of the quantum well confines electron carriers using conduction band offset.

4. The method of claim 1 wherein an electronic band structure at a hetero-junction interface of the quantum well confines hole carriers using valence band offset.

5. The method of claim 1 further comprising:
forming a graded transitional layer over a substrate; and
forming a relaxed film epitaxial layer over the transitional layer.

6. The method of claim 5 wherein the forming of the transitional layer and the relaxed film epitaxial layer reduce a dislocation defect of the quantum well layer.

7. The method of claim 5 further comprising forming a first Si1-yGey layer over the relaxed film epitaxial layer.

8. The method of claim 7 further comprising forming the quantum well over the first Si1-yGey layer.

9. The method of claim 8 further comprising:
forming a first diffusion barrier over the quantum well;
forming a second Si1-yGey layer over the first diffusion barrier; and
forming a second diffusion barrier over the second Si1-yGey layer.

10. The method of claim 7 further performing Complementary Metal-Oxide Semiconductor (CMOS) processing to complete the fabrication of the quantum well device.

11. A quantum well semiconductor device comprising:
a quantum well;
a delta layer; and
a first diffusion barrier formed below the delta layer; and
a second diffusion barrier formed above the delta layer.

12. The device of claim 11 further comprising:
a substrate;
a graded transitional layer formed over the substrate; and
a relaxed film epitaxial layer formed over the transitional layer.

13. The device of claim 12 wherein the transitional layer and the relaxed film epitaxial layer are formed to reduce a dislocation defect of the quantum well layer.

14. The device of claim 5 further comprising a first Si1-yGey layer formed over the relaxed film epitaxial layer and below the quantum well.

15. The device of claim 11 wherein an electronic band structure at a hetero-junction interface of the quantum well confines electron carriers using conduction band offset.

16. The device of claim 11 wherein an electronic band structure at a hetero-junction interface of the quantum well confines hole carriers using valence band offset.

forming a relaxed film epitaxial layer over the transitional layer;
forming a first Si1-yGey layer over the relaxed film epitaxial layer;
forming the quantum well over the first Si1-yGey layer.
forming a first diffusion barrier over the quantum well;
forming a second Si1-yGey layer over the first diffusion barrier; and
forming a second diffusion barrier over the second Si1-yGey layer.

18. The method of claim 17 further performing Complementary Metal-Oxide Semiconductor (CMOS) processing to complete the fabrication of the quantum well semiconductor device.

19. The method of claim 17 wherein an electronic band structure at a hetero-junction interface of the quantum well confines electron carriers using conduction band offset.

20. The method of claim 17 wherein an electronic band structure at a hetero-junction interface of the quantum well confines hole carriers using valence band offset.