

CLAIMS

1. A method for detecting perturbations (1) in a logic circuit (10) for processing data operations along a plurality of datapaths (5) coordinated by a clock signal (4), at least one datapath (5) having an operating propagation delay,
- 5 said logic circuit (10) further comprising at least one test circuit (21, 21') having a programmable length datapath (22) for varying a test propagation delay (2'), said test circuit (21, 21') comprising inputs (X, Y), to be processed to provide an output (N) at an instant depending on the programmable length datapath (22), and an error generator (26) for providing an error (E) in case that the output (N) is
- 10 different than an expected output (R1, R2) for said inputs (X, Y), said test circuit (21, 21') being configured to operate in two modes, a calibration mode (Mc) and a detection mode (Md), so as repeatedly switching between said modes (Mc, Md), said calibration mode (Mc) comprising:
- determining a critical propagation delay by varying the programmable length
 - 15 datapath (22) until the error generator (26) outputs an error (E),
 - adjusting the programmable length datapath (22) to include therein a tolerance delay (3'),
 - switching into detection mode (Md),
- said detection mode (Md) comprising:
- 20 - detecting a perturbation (1) in the logic circuit (10) along the programmable length datapath (22) in case the error generator (26) outputs an error (E).
2. The method of claim 1, wherein the logic circuit (10) further comprises a second test circuit (21'), said second test circuit (21') having at least the same
- 25 capabilities as the first test circuit (21), and wherein when one test circuit (21, 21') is in one mode (Mc, Md), the other one is in the other mode.
3. The method of claim 1 or 2, wherein varying the programmable length datapath (22), for determining said critical propagation delay, is stopped before said
- 30 critical propagation delay is lower than a minimum delay for processing said data operations without perturbation (1).

4. The method of any of preceding claims, wherein said method comprises iterations (i) for iterating over time said determining, said adjusting, said switching and said detecting.
- 5 5. The method of any of preceding claims, wherein said programmable length datapath (22) is formed by a plurality of elements (23) to be included within one clock cycle (T).
6. The method of claim 5, wherein said elements are included according to
10 a constant number during first iterations before increasing the number of elements to be included at next iterations.
7. The method of any of preceding claims, wherein switching from the calibration mode (Mc) to the detection mode (Md) is performed as soon as the
15 calibration mode (Mc) is completed.
8. The method of any of preceding claims, wherein said inputs (X, Y) of the test circuit (21, 21') are swapped or changed in order to get different outputs (N) between two successive outputs.
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9. The method of any of preceding claims, wherein the test propagation delay (2') is adjusted by applying a useful skew (t_1-t_1) to a clock branch (4') coordinating the datapath (5) generating said test propagation delay (2').
- 25 10. A logic circuit (10) for implementing the method of any of claims 1 to 9 while processing data operations along a plurality of datapaths (5) coordinated by a clock signal (4), comprising at least one test circuit (21, 21') configured to operate according to a calibration mode (Mc) and a detection mode (Md), said calibration mode (Mc) being designed to determine a critical propagation delay of a digital
30 signal (2) through at least one of said datapaths (5), and said detection mode (Md) being designed to detect a perturbation (1) in the logic circuit (10), said test circuit (21, 21') comprising:
- first registers (12a, 12b) configured to be loaded with inputs (X, Y),

- a logic unit (24) storing a function (F) configured to provide an output (N) from the inputs (X, Y),
 - second registers (12c, 12d) for storing expected outputs (R1, R2) provided by the function (F) for said inputs (X, Y),
 - 5 - a comparator (25) configured to verify whether the output (N) is equal to one of the expected outputs (R1, R2),
 - an error generator (26) for outputting an error (E) in case the comparator (25) provides a negative event,
 - a programmable length datapath (22) for varying a propagation delay (2') of the
 - 10 digital signal (2) allowing to get the output (N) from the input (X, Y), and
 - a switching unit for switching calibration mode (Mc) into detection mode (Md) and for switching detection mode (Md) into calibration mode (Mc).
11. The logic circuit (10) of claim 10, further comprising a second test circuit
- 15 (21'), said second test circuit (21') having at least the same capabilities as the first test circuit (21) and being configured for simultaneously working in one of the calibration mode (Mc) and detection mode (Md).
12. The logic circuit (10) of claim 10 or 11, wherein the programmable length
- 20 datapath (22) comprises a plurality of selectable delay cells (23).
13. The logic circuit (10) of any of claims 10 to 12, wherein it is limited to fully digital components.