SPECIFICATION
Integrated logic circuits

The invention relates to integrated logic circuits having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled via a diode to a collector of the bipolar transistor.

Pages 168 and 169 of the Digest of Technical Papers, February 1975 of the "1975 I.E.E.E. International Solid-State Circuits Conference" describe an integrated logic circuit having a signal input which is formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled, *via* a diode, to the collector of the bipolar transistor. The signal input comprises current supply means. The integrated circuit comprises a semiconductor body having a major surface adjoined by several surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first. Each of the said surface regions is surrounded at the major surface by an isolation zone by means of which the surface regions are isolated electrically from each other at least during operation. One of the said surface regions of the first conductivity type serves as a collector region of the bipolar transistor. Said bipolar transistor furthermore has an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and is separated from the collector region in the semiconductor body by a base zone of the second conductivity type situated above a portion of the collector region and extending up to the major surface. The base zone forms a first *p-n* junction with said emitter zone, and forms a second *p-n* junction with the collector region. An electrically insulating layer is present on the major surface and has a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and several third apertures which are situated beside the base zone and above the collector region. The insulating layer separates from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures. Each of the conductor tracks which extends into a third aperture is coupled to the collector region *via* a rectifying junction which adjoins the collector region.

This circuit known from the said "Digest of Technical Papers" is described as being very attractive for large-scale integrated logic circuits (LSI). The basic cell is a NAND gate in which the coupling diodes at the signal outputs are provided as Schottky diodes. In addition the cell also comprises a Schottky diode which is connected in parallel with the collector-base junction of the transistor. This latter Schottky diode (clamp diode) has a diode forward voltage differing from that of the coupling diodes. The swing of the logic signal (that is the voltage difference between the signals representing a logic 1 and a logic 0, respectively) equal to the difference in diode forward voltage of the two mutually different types of Schottky diodes. As a result, this swing can be comparatively small, which improves the switching speed of the cell. The minimum delay time of the cell is comparable to that of the transistor-transistor logic version with Schottky diode clamping and low dissipation which is sometimes referred to by the abbreviation LS TTL. Furthermore, the cell is particularly compact and the product of delay time and power dissipation is also attractively low.

Although this attractive LSI logic was announced nearly three years ago now, it has up till now not resulted in commercial products which have found acceptance in the market, at least in as far as the inventor is aware.

The present invention is *inter alia* based on a realization by the inventor that the manufacture can be simplified considerably by modification of the integrated circuit described and, also as a result of this, the cost-price can be reduced considerably, while the attractive electrical properties and the high packing density desired for integration can be maintained for the greater part.

Surprisingly the Applicants have found experimentally that, by means of special measures in the semiconductor structure which need not require any extra operations during the manufacture, an auxiliary transistor coupled to the bipolar switching transistor can be realized which makes it possible to omit the clamp diode without the switching speed of the cell being reduced in an inadmissible manner.

According to a first aspect of the invention, there is provided an integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled *via* a diode to a collector of the bipolar transistor, the signal input comprising current supply means, and the integrated circuit comprising a semiconductor body having a major surface adjoined by several surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first, each of the said surface regions being surrounded at the major surface by an isolation zone by means of which the surface regions are isolated electrically from each other at least during operation, one of the said surface regions of the first conductivity type serving as a collector region of the bipolar transistor, said bipolar transistor furthermore having an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and is separated from the collector region in the semiconductor body by a base zone of the second conductivity type extending up to the major surface, which base zone is situated above a portion of the collector region and forms a first *p-n* junction with the said emitter zone and a second *p-n* junction with the collector region, an electrically insulating layer being present on the major surface and having a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and

third apertures which are situated beside the base zone and above the collector region, the insulating layer separating from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures, each of the conductor tracks which extends into a third aperture being coupled to the collector region *via* rectifying junction which adjoins the collector region, characterized in that an additional measure has been taken in the semiconductor structure of the bipolar transistor as a result of which a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone and collector region of said bipolar transistor so that a complementary auxiliary transistor is incorporated which has the said base zone of the second conductivity type as emitter, has the collector region of the first conductivity type as base and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

According to a second aspect of the invention, there is provided an integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled via a diode to a collector of the bipolar transistor, which transistor has an emitter zone of a first conductivity type and a base zone of a second conductivity type opposite to the first, the signal input comprising current supply means, the integrated circuit comprising in a semiconductor body a semiconductor region of the first conductivity type which belongs to a collector region of the bipolar transistor and is situated on a substrate region of the second conductivity type, the base zone being situated above a portion of the collector region, characterized in that an additional measure has been taken in the semiconductor structure of the bipolar transistor as a result of which a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone and collector region of said bipolar transistor so that a complementary auxiliary transistor is incorporated which has the said base zone of the second conductivity type as emitter, has the collector region of the first conductivity type as base and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the auxiliary transistor and the storage of mobile charge carriers in the over driven bipolar transistor can be restricted considerably.

Such integrated logic circuits in accordance with the invention with an inverter transistor having coupling diodes on or in the collector region and an effective build-in complementary auxiliary transistor can provide a considerable improvement with respect to LS TTL. The switching speed of the gate circuit can be at least equal to that of LS TTL while the power consumption can be considerably smaller; the packing density may be in addition approximately a factor to two to six larger. It is important that this improvement can be realized without necessitating a very complicated manufacturing process. The manufacturing process necessary for the proposed integrated circuit can involve the same process steps which are used for LS TTL. It is therefore important and surprising that by means of the present invention such a considerable improvement with respect to LS TTL can be realized.

In an important form in accordance with the invention the complementary auxiliary transistor is realized (at least partly) as a vertical transistor. Thus, the collector region of the first conductivity type may have a high-ohmic part and a low-ohmic part which extends at and along the interface between the collector region and the substrate, and this embodiment may be further characterized in that the extent of the low-ohmic part of the said collector region in a direction substantially parallel to the major surface is restricted so that said low-ohmic part extends below the said emitter zone and below the rectifying junctions of the signal-output diodes but does not extend below part of said base zone underlying the second aperture in the insulating layer whereby a region of the high-ohmic part of the collector region directly adjoins the substrate region to form a third *p-n* junction, the part of the substrate region adjoining the high-ohmic part of the collector region co-operating as a collector of the auxiliary transistor with the adjoining collector region and the base zone of the bipolar transistor. The thickness of the high-ohmic part of the collector region measured between the second and the third *p-n* junction is then preferably at most 5 microns.

Such a vertical auxiliary transistor which causes excessive base current of the inverter transistor to flow away *via* the substrate region proves to be a particularly effective means to restrict the overdrive of the inverter transistor and to reduce the storage of mobile minority charge carriers in said transistor so that comparatively short switching times are realized.

In another important form in accordance with the invention the complementary auxiliary transistor is incorporated (at least partly) as a lateral transistor. This embodiment may be characterized in that a further surface zone of the second conductivity type adjoining the collector region of the first conductivity type is present at the major surface and beside the base zone and extends into the semiconductor body from the major surfaced down to substantially the same depth as the base zone, said further zone serving as a collector of the auxiliary transistor and being connected to the substrate region.

Said further surface zone can simply be

provided simultaneously with the base zone so that the distance between said zones can be comparatively small. The distance at the major surface between the base zone and the further surface zone is preferably at most 5 microns (5×10^{-6} metres).

The vertical and the horizontal auxiliary transistor may also be combined advantageously in the same bipolar transistor of an integrated circuit in accordance with the invention.

Embodiments of the invention will be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is the electrical circuit diagram of the known NAND gate;

Figure 2 is a part of a diagrammatic plan view of a first integrated circuit in accordance with the invention;

Figures 3 and 4 are diagrammatic cross-sectional views of said part of the first circuit taken on the lines III—III and IV—IV, respectively, of Figure 2;

Figure 5 shows diagrammatically a part of a second integrated circuit in accordance with the invention, and

Figure 6 is a diagrammatically cross-sectional view of said second circuit taken on the line VI—VI of Figure 5.

The electrical circuit diagram of the above-mentioned known NAND gate, shown in Figure 1, has a signal input 1 which is formed by the base of a bipolar transistor T and several signal outputs 2, 3, 4 and 5 which are each coupled to the collector of the bipolar transistor T *via* a diode 6. The signal input 1 has current-supply means which are denoted by the current source 1.

The transistor T is a planar transistor, the collector-base junction of which is shunted by a Schottky diode 7. Due to said clamp diode the transistor has the high switching speed which is desired nowadays for logic circuits. If the clamp diode 7 is omitted, the transistor in the conductive state will become highly saturated. The transistor then comprises a large amount of stored charge, mainly in the form of minority charge carriers, which are situated in the collector region. The switching-off of the transistor would then occur only slowly. The clamp diode 7 prevents the transistor from becoming saturated so that this charge storage is avoided.

If during operation the signal input 1 is not connected, the signal input 1 will be charged by the supplied current I to the emitter-base voltage of the transistor T associated with the conductive state. This diode forward voltage or junction voltage V_{BE} is, for example, approximately 700 to 750 mV for a silicon transistor.

When the voltage at the signal input reaches the diode forward voltage V_{BE}, the transistor T becomes conductive and the current I is used as a base current. The current available at one or more of the signal outputs is then dissipated *via* transistor T, the voltage at the relevant signal output being equal to the diode forward voltage V_{D1} of the coupling diodes 6 augmented by the collector-emitter voltage of the conductive transistor T. This collector-emitter voltage is equal to the voltage V_{BE} reduced by the diode forward voltage V_{D2} of the clamp diode 7. If the voltage V_{D2} is larger than the voltage V_{D1}, the signal output voltage is smaller than V_{BE} and the transistor of a following NAND gate connected to the relevant signal output will be kept in the non-conductive state.

The swing of the logic signal, that is the difference between the high and the low signal level, is equal to the difference between the diode forward voltages V_{D2} of the clamp diode 7 and V_{D1} of the coupling diode 6.

The Schottky clamp diode is a PtSiSi contact with a diode forward voltage V_{D2} of approximately 500 mV. The Schottky coupling diodes 6 are TiSi contacts with a diode forward voltage of approximately 350 mV. The logic swing is then approximately 150 mV. This comparatively small logic swing has a favourable effect on the delay time of the gate circuit. When switching from the high to the low signal state, or conversely, only a small voltage difference need be bridged. So the switching can be realized in a correspondingly short period of time.

Thus, the described known logic circuit owes its attractive circuit properties to two things. In the first place there is the use of a high speed planar transistor T which is freed from saturation by means of the Schottky diode 7, and in the second place there are the metal-to-semiconductor contacts having different compositions of metallization which provide Schottky diodes with a favourably small difference in diode forward voltage of approximately 150 mV. Hence both in the switching transistor T and in determining the desired logic swing the metallization chosen plays an essential decisive part.

The present invention makes it possible to use, instead of this choice of complex metallization which necessarily is constructed from conductive layers of different materials, a much simpler metallization which may, for example, have been used already in existing products.

The first embodiment which will be described further with reference to Figures 2, 3 and 4 has a semiconductor body 20 a major surface 21 of which is adjoined by several surface regions 22 to 28 of a first conductivity type which are situated on a common substrate region 29 of a second conductivity type opposite to the first. The substrate region 29 may be a semiconductor layer provided, for example, on any suitable substrate. In the present example the region 29 is a *p*-type semiconductor substrate of silicon having a resistivity of, for example, 10 to 15 ohm-cm.

At the major surface 21 of the surface regions 22 to 28 are each surrounded by an isolation zone 30 by means of which the surface regions are isolated electrically from each other at least during operation. The isolation zones may consist entirely or partly of insulating material. Alternatively, *p*-type zones may be used extending from the major surface 21 into an *n*-type surface layer. The *p*-type

isolation zones 30 extend over a part of the thickness of the surface layer or penetrate through the surface layer entirely so that they reach down into the substrate 29, as illustrated in Figures 3 and 4. By applying a voltage in the reverse direction across the *p-n* junctions formed between the isolation zones 30 and the surface regions 22 to 28 and between the substrate 29 and the surface regions 22 to 28, electric isolation between the surface regions 22 to 28 can be ensured in the usual manner during operation.

As illustrated by region 22 in Figure 3, at least one of the surface regions 22 to 28 serves as a collector region of a bipolar transistor. This collector region 22 has a high-ohmic part 31 and a low-ohmic part 32. The low-ohmic part 32 extends at and along the interface between the collector region 22 and the substrate region 29.

The bipolar transistor furthermore has an emitter zone 33 of the first conductivity type which adjoins the major surface 21 and which is separated in the semiconductor body 20 from the collector region 22 by a base zone 34 of the second conductivity type extending up to the major surface 21. The base zone 34 is situated above a portion of the collector region 22. The *n*-type emitter zone 33 forms, with the *p*-type base zone 34, a first *p-n* junction 35 having a first diode forward voltage V_{BE}. The *p*-type base zone 34 forms, with the *n*-type collector region 22, a second *p-n* junction 36.

Present on the major surface 21 is an electrically insulating layer 37 which in the plan view shown in Figure 2 is considered to be transparent. The layer 37 consists of an insulating material, for example silicon dioxide or silicon nitride or a combination thereof. A first aperture 38 in the insulating layer 37 is situated above the emitter zone 33. A second aperture 39 is situated beside the emitter zone 33 and above the base zone 34. In addition, beside the base zone 34 and above the collector region 22 several third apertures 40 are present. In Figure 2, the apertures shown in the insulating layer 37 are illustrated with a cross.

The insulating layer 37 separates conductor tracks 11, 12, 13, 14, 15 and 41 from the semiconductor body 20; these tracks extend into the first, second and third apertures 38, 39 and 40, respectively, for the electrical connection. For clarity, no conductor tracks are drawn in Figure 2.

The conductor tracks 12, 13, 14 and 15 extending into the third apertures 40 are each coupled to the collector region 22 *via* a rectifying junction 16 which adjoins said collector region. In this example the rectifying junctions 16 are metal-to-semiconductor junctions or Schottky junctions. These Schottky junctions may be formed as platinel silicide contacts as described in, for example, United States Patent Specification US—PS 3,855,612. The rectifying junctions 16 have a diode forward voltage V_{D1}. For the operation of the circuit it is desirable that junctions 16 used have a diode forward voltage V_{D1} which is smaller than the diode forward voltage V_{BE} of the emitter-base *p-n* junction 35 of the transistor.

In accordance with the invention, the extent of the low-ohmic part 32 of the collector region 22 in a direction substantially parallel to the major surface 21 is restricted so as to form a complementary auxiliary transistor. The region 32 extends below the emitter zone 33 and below the rectifying junctions 16 but does not extend below part of the base zone 34 underlying the second aperture 39; in this way a region of the high-ohmic part 31 of the collector region directly adjoins the substrate region 29 to form a third *p-n* junction 42. The thickness of the high-ohmic part 31 of the collector region 22 measured between the second and third *p-n* junctions 36 and 42, respectively, is preferably smaller than 5 microns. As a result of this, a vertical complementary (*p-n-p*) auxiliary transistor the emitter of which is formed by the base zone 34, the base of which is formed by the high-ohmic part 31 of the collector region 22 between the *p-n* junctions 36 and 42, and the collector of which is formed by the substrate region 29, is incorporated in the *p-n-p* transistor structure in an effective manner and substantially without this requiring more semiconductor surface area for the transistor. In this example the extent of the buried layer 32 is made smaller than is usual so that below the base contact the substrate region extends up to a comparatively small distance from the base-collector junction 36; by taking such an additional measure the relevant part of the substrate region co-operates effectively as collector of the complementary auxiliary transistor with the adjoining high-ohmic part 31 and the base zone 34. As a result of this, when the inverter transistor is overdriven a considerable part of the current flowing in the base zone 34 flows through the auxiliary transistor and the storage of mobile charge carriers in the overdriven inverter transistor is restricted considerably, as will be explained hereinafter.

Figure 2 also shows surface regions 33 to 27 which comprise identical, at least similar circuit elements. So said regions each serve as a collector region of a planar *n-p-n* transistor having a number of signal output tracks which are coupled to the relevant collector region *via* a diode. The number of diodes may vary for each individual transistor between one and, for example, four or five and will depend on the logic function to be generated by the integrated circuit.

The collector regions or islands 22 to 27 are arranged on both sides of an elongate surface region 28 from which the signal inputs 11 are provided with current. In this region 28 a number of lateral *p-n-p* transistors are provided which have a common *p*-type emitter zone 43. The region 28 serves as a common *n*-type base zone. The *p-n-p* transistors each have a separate *p*-type collector zone 44 which is connected to a signal input 11 *via* an aperture 45 in the insulating layer 37. The common emitter zone 43 is connected, *via* an aperture 46, to a conductor track 47 which has a diagrammatically shown connection 48 for a

supply source.

The common base zone 28 has a high-ohmic part 49 and a low-ohmic part 50 in the form of a buried layer. Furthermore, a low-ohmic *n*-type surface region 51 is present in the base zone 28 which may be provided, for example, simultaneously with the emitter zone 34 and which screens the individual collector zones 44 from each other at least partly. In a corresponding manner the region 51 also constitutes a screening between the emitter and collector zones on the one hand and the isolation zones 30 on the other hand. The buried layer 50 and the surface region 51 serve to reduce the base series resistance and to suppress parasitic transistor action to the substrate and/or the isolation zones and between the collector zones mutually. Above the surface region 51 there are apertures 52, 59 in the insulating layer 37 through which the common base zone 28 is connected to conductor tracks 53.

The integrated circuit is constructed with a metallization which comprises several layers, as is common for complex LSI circuits nowadays. For that purpose, the insulating layer 37 consists of a first or lowermost layer 55 having the apertures 38, 39, 40, 45, 46 and 52 and a second or uppermost layer 56. A first level of conductor tracks which comprises *inter alia* the conductor tracks 11 to 15 and 47 is situated on the lowermost layer 55. The conductor tracks 41 and 53 consist of two parts of which first parts 57 and 63, respectively lie at the first level and extend into the apertures 38 and 52, respectively, and second parts 58 and 64, respectively lie on a second level which is separated from the first level by the uppermost layer 56; the second parts 58 and 64 are directly connected to the first parts 57 and 63, respectively, *via* apertures 59.

The second parts 64 of the conductor tracks 53 are, for example, comb-shaped, the base of the comb extending substantially parallel to the emitter zone 43 and the conductor tracks 47, and projections or teeth of the comb extending from the base of the comb towards and into the apertures 59 in the insulating layer 37. The second parts 64 may also be connected to a connection 54, shown diagrammatically, for the conductor tracks 53.

The conductor tracks 11 to 15, 47 and 57 of the first level may be, for example, aluminium or another suitable conductive material. If desired, a barrier layer may be used to avoid direct contact between the aluminium and the platinel silicide formed in the apertures in the insulating layer. As a barrier layer may be used, for example, titanium-platinum or titanium-tungsten or rhodium.

The conductor tracks 58 and 64 of the second level are, for example, of aluminium or titanium-platinum-gold.

Preferably, the same material is in direct contact with the semiconductor body in all apertures 38, 39, 40, 46 and 52 in the first insulating layer 37, and particularly in the first, the second and the third apertures 38, 39 and 40. In the present example, this material is the said platinel silicide which in the apertures 40 forms a Schottky diode and which, in the other apertures, forms a readily conductive junction between the conductor tracks and the adjoining semiconductor regions in said apertures.

The conductor track 41 connected to the emitter zone 33 is provided with a connection 60, shown diagrammatically, and the substrate region 29 has a connection 61 which may be connected to the connection 60 to form a common connection 62 for a supply source.

The connection 62 may be connected to a suitable reference potential, for example earth potential. A suitable current or voltage supply source is connected between the connections 62 and 48. The connection 54 is connected to a suitable reference potential, the *p-n-p* transistors being conductive. The integrated circuit furthermore has one or more signal inputs, not shown, *via* which input signals can be supplied to one or more conductor tracks 11, and one or more signal outputs, not shown *via* which output signals generated by the integrated circuit can be derived. For the sake of completeness it is noted that the second level of conductor tracks may be covered entirely or partly with a further insulating layer, if so desired.

The embodiment described has a combination of properties which are particularly suitable for LSI circuits. First of all, the manufacturing process necessary for this integrated circuit is considerably simpler than for the described known circuit. This integrated circuit in accordance with the invention can be manufactured with the same available process steps by which, for example, LS TTL and I^2L can also be manufactured. In contrast with the known circuit described, LS TTL and I^2L are both on the market as commercial products. Comparison of the integrated circuit in accordance with the invention with these two commercial products can provide a convenient assessment of the particular suitability and applicability of the new LSI logic circuit in accordance with the invention. In such a comparison it is not only of importance that the products to be compared should be manufactured in the same or substantially the same process but also that comparable design rules for the topology or lay-out should be used. The results to be mentioned hereinafter are based on a comparison in which for all three products it has been assumed that the smallest details to be realized in the masks must have a length of at least 5 microns. Furthermore, an *n*-type epitaxial layer in a thickness of approximately 3 microns and a resistivity of approximately 0.7 ohm-cm was used for the circuit in accordance with the invention. As stated, the Schottky coupling diodes were of a type which is also usual in LS TTL having a platinel silicide junction. The diode forward voltage of said diodes was approximately 0.48V.

As is known, the conventional I^2L is comparatively slow as compared with LS TTL. The minimum delay time of an I^2L inverter having a single output is approximately 10 to 20

nanoseconds (nsec) whereas for LS TTL the minimum delay time is in the proximity of approximately 5 to 7 nanoseconds (nsec). The switching times given here are realized in I^2L and LS TTL integrated circuits, respectively, with an epitaxial layer having a thickness of approximately 3 microns. The resistivity of the epitaxial layer for I^2 circuits is approximately 0.7 ohm-cm, whereas for LS TTL circuits a value of approximately 0.3 ohm-cm has been assumed.

It is very surprising that the minimum delay time for the circuit in accordance with the invention is approximately 3 to 3.5 nsec. This minimum delay time was measured at a current level of approximately 400 microAmps (μA). The emitter-base-diode forward voltage was approximately 760 milliVolts (mV) and the collector-emitter voltage V_{CE} of the conductive inverter transistor was approximately 60 mV. The swing of the logic signal was approximately 220 mV.

In spite of the fact that the inverter transistor in LS TTL is kept from saturation by means of a Schottky clamp diode and the inverter transistor in the circuit in accordance with the invention does become saturated, the latter circuit nevertheless has a delay time which is approximately half as short. The comparable I^2L inverter which also becomes saturated has on the contrary a 3 to 6 times longer delay time. Apparently, the restriction of the extent of the buried layer as indicated is an unexpectedly effective means in which on the one hand the internal series resistance in the collector region is not increased or is hardly increased, while on the other hand a particularly effective complementary auxiliary transistor is obtained which drastically reduces the consequences of the fact that the inverter transistor becomes saturated and which readily controls the extent to which the inverter transistor becomes saturated.

Another quantity which is frequently used for comparison is the product of the delay time τ and the power dissipation D. For LS TTL this τ.D product is approximately 19 pJ, for I^2L and the circuit according to the invention the τ.D product is of approximately the same value, namely 0.5 to 2 pJ. So the integrated circuit in accordance with the invention also compares well in this respect.

A third quantity which is extremely important for LSI circuits is the packing density or the number of gate circuits which can on average be realized per mm^2 of semiconductor surface area. In this respect, as is known, I^2L with a packing density of approximately 200 to 250 gates per mm^2 is superior to LS TTL which has a packing density of 15 to 20 gates per mm^2. The packing density of the integrated circuit in accordance with the invention is 120 to 180 gates per mm^2; this is approximately a factor of 6 more favourable than for LS TTL and less than a factor of 2 worse than for I^2L.

Thus, the present invention can provide a considerable improvement with respect to LS TTL, and the resulting circuit can be of advantage with respect to I^2L for applications in which a switching speed is necessary which is too high for conventional I^2L. InI^2L switching speeds of a few nanoseconds can be realized in practice only if dielectric isolation is used; however, the associated manufacturing process is more complicated that the conventional manufacturing process so that a comparatively high cost-price results. Furthermore, for corresponding reasons as is the case with I^2L, the switching speeds in an integrated logic circuit in accordance with the invention can also be increased by using dielectric isolation.

In the second embodiment which will be described with reference to Figures 5 and 6, a number of further measures have been taken to improve the integrated circuit. In this example, the same reference numerals are used as in the first example, the same reference numerals are used as in the first example for corresponding parts, particularly of the inverter transistor and the coupling diodes.

In the plan view of Figure 5 some of the conductor tracks at the first level are shown. They are, *inter alia*, the conductors 11, 12 and 57. For clarity, the conductor tracks shown are shaded.

A first measure to improve the switching speed is that the non-active part of the base zone 34 is enlarged and is significantly larger than is necessary for providing a base contact, while nevertheless the extent of the buried layer 32 is restricted to the region below the emitter zone 33 and the active part of the base zone 34.

The active part of the base zone 34 is to be understood to mean in this connection that part which is necessary to accommodate an emitter zone 33. Adjoining said active part, a non-active part of the base zone 34 is necessary for the electrical connection of the conductor track 11.

If in the present examples an emitter zone 33 of, for example, 12 microns x 12 microns with an associated contact aperture 38 of approximately 6 microns x 6 microns is used and a minimum of 3 microns is maintained for the distance at the semiconductor surface between the emitter-base junction 35 and the base-collector junction 36, the active part of the base zone necessary for the emitter zone is 18 microns x 18 microns. However, at least one contact aperture for contacting the base is necessary beside the emitter zone. Said contact aperture 39 is, for example, 5 microns x 10 microns. If in addition a minimum distance of approximately 6 microns between the conductors 57 and 11 extending into the apertures 38 and 39 is taken into account, the base zone 34 as a whole will be 18 microns x 32 microns. The non-active part of the base zone 34 destined for contacting hence is at least 18 microns x 14 microns. With the dimensions indicated, the non-active part has a surface area which is more than 20% smaller than the active part.

In the present second example a base zone 34 is used of 37 microns x 18 microns having therein the same emitter zone of 12 microns x 12

microns. So in this case the active part also has an area of 18 microns x 18 microns. The non-active part in this case measures 18 microns x 19 microns. In this second example the non-active part hence is approximately 35% larger in area than in the first example. In addition, the non-active part in this second example even has a larger area than the active part. Within the scope of the present invention, the non-active part of the base zone 34 which provides the emitter of the vertical complementary auxiliary transistor is preferably at least equally large as the active part.

In the second example, the larger base zone 34 is used to enlarge the contact aperture 39. Instead of an aperture of 5 microns x 10 microns, an aperture 39 of 10 microns x 10 microns is used in this case. So the aperture 39 is twice as wide as is minimally necessary. In itself this widening of the aperture 39 is not necessary for the good operation of the integrated circuit. Independently of the aperture 39 actually present, the extension of the base zone 34 as proposed within the scope of the present invention will preferably be of such a nature that the non-active part of the base zone 34 is so large that sufficient area is available to be able to use a contact aperture 39 having a width which is larger than the smallest dimension of the apertures 40 for the coupling diodes. The available area is preferably sufficiently large for a contact aperture having a width which is at least equal to twice the smallest dimension of the apertures 40. In the two examples the apertures 40 have dimensions of 5 microns x 22 microns.

For completeness' sake it is to be noted that the above-indicated dimensions relate for simplicity to the masks which are necessary for the various photolithographic treatments during the manufacture. As is known, the actual dimensions in the integrated circuits themselves differ slightly *inter alia* because upon exposure and development of the photosensitive lacquer an exact reproduction of the masks is not obtained, because during the etching treatments undercutting often occurs and because upon diffusion of impurities, lateral diffusion also occurs.

As a result of the indicated enlargement of the base zone 34, the oppositely located parts of the *p-n* junctions 36 and 42 also obtain a larger area. So in fact the incorporated vertical *p-n-p* auxiliary transistor is enlarged as a result of which excessive base current of the conductive inverter transistor can be dissipated more effectively and at a lower forward voltage across the *p-n* junction 36. The conductive inverter transistor is overdriven less and the storage of charge in the collector region 22 is accordingly reduced.

In the above paragraphs it is assumed that the inverter transistor has a single emitter zone 33 and a single base contact aperture 38. Dependent *inter alia* on the desired current level, for example, two conductively interconnected emitter zones may also be used. Alternatively, several base contact apertures may be present, for example, two contact apertures on oppositely located sides of a single emitter zone. When several base contact apertures are used, an auxiliary transistor need not necessarily be incorporated below each of the base contacts. The collector region 22 of the inverter transistor preferably is substantially rectangular and the apertures 38, 39 and 40 in the insulating layer are situated beside each other in the same direction, the aperture of apertures 39 and the associated emitter zone or zones 33 being situated between the apertures 40 for the coupling diodes on one side and the or at least one of the apertures 38 for the base contact on the other side. The desired incorporated vertical auxiliary transistor is preferably situated below the last-mentioned outermost contact aperture. The buried layer 32 preferably continues uninterruptedly from below the emitter zone 33 to below the coupling diodes 16.

A further measure to improve the switching speed is that an improved lateral auxiliary transistor is incorporated by the addition of a further surface zone 71 which during the manufacture can be obtained simultaneously with the base zone 34. The zone 71 has the same conductivity type as the base zone 34 and as the isolation zone 30 and at the semiconductor surface coincides partly with the isolation zone 30. The zones 71 and 30 overlap each other. The base zone 34 and the isolation zone 30 are obtained with different diffusion treatments so that their mutual distance can be comparatively small. They have substantially the same depth of penetration in the semiconductor body and they have substantially the same variation in doping concentration in a direction transverse to the major surface. A usual distance between the base zone 34 and the isolation zone 30 would be, for example, approximately 10 microns. The distance between the base zone 34 and the further surface zone 71 need not be more than 5 microns. The zones 34 and 71 constitute the emitter and the collector of an effective lateral auxiliary transistor the base width of which is 5 microns or less. If the inverter transistor is conductive, said auxiliary transistor also dissipates current so that the inverter transistor is less overdriven.

As stated, the base width of the lateral auxiliary transistor is preferably at most 5 microns. In the present example the indicated distances of 10 and 5 microns apply to the masks to be used in the manufacture and the corresponding dimensions in the integrated circuit are smaller, in particular due to the occurrence of lateral diffusion. The distance between the base zone 34 and the isolation zone 30 will be on an average be approximately 7 microns. The base width of the lateral auxiliary transistor actually is approximately 3 microns.

In this embodiment having a lateral complementary auxiliary transistor the additional surface zone 71 constitutes the region of the second conductivity type which effectively serves as collector of the auxiliary transistor.

The further surface zone 71 may have a closed geometry and surround the base zone 34 as a ring which extends between the base zone 34 on the

one side and the coupling diodes 16 on the other side. Preferably, however, the further zone 71 is open on the side of the coupling diodes 16 and surrounds the base zone 34 only at the part of the edge of the base zone not facing the coupling diodes. Therefore in the present example the zone 71 is in the form of a U.

The use of a zone 71 having a non-closed geometry is based on the realisation of the fact that such a zone is substantially superfluous on the side of the base zone 34 facing the coupling diodes 16. Particularly if the coupling diodes are Schottky diodes, the lifetime of the minority charge carriers in the collector region 22 at the rectifying junctions 16 is very small. In particular the first coupling diode situated nearest the base zone 34 will draw minority charge carriers from the collector region and thus fulfills substantially the same function as the zone 71. As a result of this, a slightly larger current will flow through the first coupling diode than through the remaining coupling diodes which are situated farther away. The difference in current level, however, is so small that the proper electrical operation of the circuit is not endangered. The inverter transistors have amply sufficient gain to be able to absorb said current differences.

The U-shape selected for the further surface zone 71 has the important advantage that no extra area is necessary at the semiconductor surface. A closed shape or ring surrounding the whole collector region would restrict the area available for the coupling diodes. A closed shape or ring surrounding the base zone 34 and extending between the base zone 34 and the first coupling diode 16 would necessitate a larger distance between said base zone 34 and the first coupling diode 16.

Another measure by which the switching speed can be increased is to replace the lateral *p-n-p* transistor 46, 28, 45 of the first example used for the supply of current by a resistor in combination with an as low as possible supply voltage of 1V or less. The supply voltage preferably is at most equal to the sum of the diode forward voltage V_{BE} of the inverter transistor and the swing of the logic signal, or in other words, at most equal to approximately $2V_{BE}—V_{D1}$, where V_{D1} is the diode forward voltage of the coupling diodes.

The last-mentioned measure has also been realized in the second example. The collector regions 22 to 26 of the inverter transistors are arranged on the oppositely located sides of a common surface region or island 72. Said island 72 comprises a number of resistors 73 which are each connected to a signal input conductor 11. The resistors 73 furthermore comprise connection contacts in the form of a conductive layer 74 which, as the conductive layers 57 connected to the emitter zone 33, belong to the first level of conductor tracks. The conductive layers 74 serve for the connection to a supply line 75 which is not shown in Figure 5 and extends horizontally in the plane of the drawing of Figure 5 substantially centrally above the resistors 73. This horizontal supply line 75 belongs to the conductor tracks of the second level and has projections which in the plane of Figure 5 are directed alternately upwards and downwards and which are connected to the layers 74 through an aperture in the insulating layer 56 which separates the conductor tracks of different levels from each other.

The second supply line 58 also belongs to the conductor tracks of the second level and is not shown in the drawing of Figure 5. The supply line 58 extends substantially parallel to the supply line 75 and overlies the emitter zone 33.

Finally Figure 5 shows a few signal input conductors 11 and signal output conductors 12 which belong to the first level of conductor tracks. In so far as signals of other parts of the integrated circuit situated farther away are to be supplied to the inverter transistors shown, at least two positions situated between the electrical connections of the resistors 73 in a direction parallel to the supply lines are available. In addition, a position may sometimes be used between the resistors and the inverter transistors as is shown at the bottom of Figure 5. Furthermore, signal conductors crossing each other can also be realized by means of the second level of conductor tracks.

The resistors 73 have a structure which is usual for integrated circuits. They are *p*-type zones which can be obtained simultaneously with the base zones 34. Said zones 73 are situated in the common island 72 above a buried layer 76 belonging to the island 72. A more highly doped *n*-type surface zone 77 is provided at the end of the resistors 73 connected to the supply line 75, simultaneously with the emitter zones 33. The *p-n* junction 78 formed at the boundary of the zones 73 and 77 is short-circuited by the overlying conductive layer 74. The supply line 75 is connected directly to the common island 72 *via* the surface zones 77.

It will be clear that not all resistors need be connected on one side to the common island 72 *via* an adjoining surface zone 77 and a short-circuited *p-n* junction 78. For example, one single connection between the supply line 75 and the common island 72 will in itself often suffice. Only the leakage currents of the various *p-n* junctions need be dissipated *via* the connection to the supply line, so that the current through said connection is comparatively small.

The sheet resistance of the zones 73 is, for example, approximately 200 ohm. The resistors each have a value of, for example, approximately 800 ohm.

The supply line 75 is connected to a connection 48; the supply line 58, as well as the substrate region 29, is connected to the connection 62. Between the connections 48 and 62 a supply voltage can be applied of, for example, approximately 920 mV. This voltage supply is shown diagrammatically in Figure 6 by the voltage source 79.

The selected supply voltage is equal to the sum of the diode forward voltage V_{BE} of the inverter

transistor and the logic swing. The logic swing is equal to the voltage V_{BE} decreased by the diode forward voltage V_{D1} and the collector-emitter voltage V_{CE} of the conductive inverter transistor.

During operation, the output of a first gate circuit having a conductive inverter transistor then is non-conductive. A voltage drop equal to the logic swing will occur across the resistor associated with the first gate circuit. In fact, the input signal is high and equals the base-emitter forward voltage V_{BE}. A voltage drop which is twice as large as the logic swing will occur across the resistor associated with the second gate circuit. In this case the input signal is low and is approximately equal to the sum of the diode forward voltage V_{D1} and the voltage V_{CE} of the conductive transistor. The current which flows through the second resistor and which is dissipated *via* the collector of the conductive transistor thus is approximately twice as large as the current which flows through the first resistor and which is supplied to the conductive transistor as a base current. Thus the conductive transistor clearly is less overdriven than would have been the case with a more ideal current source supply. In the latter case the base and collector currents would have been substantially equally large, while in this example as a result of the low supply voltage in combination with the resistors 73, a factor of two difference occurs. The charge storage in the inverter transistor is decreased accordingly.

Also when a higher supply voltage is used it may be of advantage to supply the currents *via* resistors to the bases of the inverter transistors. The resistance values of the resistors will then have to be larger. If necessary, the resistors may be manufactured in known manner by means of ion implantation. In that case, resistance zones having a sheet resistance of, for example, approximately 2 K.ohm can simply be obtained. Alternatively, instead of being provided in the semiconductor body, the resistors may be provided on the body, for example with a layer of resistance material, such as titanium or polycrystalline semiconductor material, obtained by deposition or otherwise.

In the examples described, current is dissipated to the connection 61 *via* the vertical and/or the horizontal complementary auxiliary transistor. This electrical connection 61 constitutes the connection to the collector of the auxiliary transistor. In order to reduce the series resistance, another arrangement may be favourable in which this connection either does not contact the substrate 29 or is connected to it not only at the lower side of the substrate; in this other arrangement, on the upper side of the semiconductor body, the deep *p*-type isolation zones 30 are connected to a conductor track and, for example, to the supply line 58 at locations situated at a regular distance from each other. If the isolation zones consist of insulating material throughout their depth or over a part of their depth, the provision of deep semiconductor zones at locations regularly arranged between or beside the gate circuits, is recommended, which zones extend from the semiconductor surface down to the substrate region and are connected at the semiconductor surface to a conductor track so that in this manner they may serve for the desired dissipation of current.

The integrated logic circuits described can be manufactured entirely in the usual manner by means of methods conventionally used in semiconductor technology.

It will be obvious that the invention is not restricted to the embodiments described but that many variations are possible to those skilled in the art without departing from the scope of this invention. For example, other semiconductor materials, such as germanium or A_{III}-B_V compounds, may be used. Furthermore, the conductivity types in the examples may be interchanged, the electric voltages and current directions being adapted accordingly. The thickness of the surface layer is preferably not larger than approximately 6.5 microns. Advantageously a thickness of at most approximately 3.5 microns is used. The surface layer will usually be an epitaxial layer but may also be obtained differently, for example, by diffusion or ion implantation. The collector regions can also be provided as separate regions by doping in a substrate of the opposite conductivity type. The resistivity or in general the doping concentration of the surface layer may be adapted within wide limits. For example, instead of the epitaxial layer of 0.7 ohm-cm an epitaxial layer of approximately 0.3 ohm-cm may alternatively be used. Such a change in resistivity influences *inter alia* the series resistance of the coupling diodes.

Both for the vertical auxiliary transistor and for the lateral auxiliary transistor, the base width of the auxiliary transistor between the emitter and the collector is preferably approximately 3 microns or less.

The inverter transistor may alternatively be constructed so as to be symmetrical with respect to the non-active part of the base zone which comprises the emitter of the auxiliary transistor. In that case the relevant base contact will be situated centrally, an emitter zone and one or more coupling diodes being present on two opposite sides of said contact. On each of the said sides a buried layer will be present which continues uninterruptedly from below the emitter zone to below the coupling diode(s). If a lateral auxiliary transistor is incorporated in such a symmetrical transistor, the region which serves as collector thereof will consist of two parts which are situated beside the two other opposite sides of the base zone not facing coupling diodes.

The active dopant concentration in the part of the substrate region which is situated as collector of the vertical auxiliary transistor opposite to the base zone of the inverter transistor, is preferably at least a factor of 10 and advantageously at least a factor of 100 lower than the active dopant concentration in the low-ohmic part of the

collector region of the inverter.

The coupling diodes 16 may be obtained by means of materials other than the said platinel silicide; thus for example, aluminium, platinum silicide or titanium may be used. This material may be present only in the apertures in the insulating layer, as with the described platinel silicide junctions, or may form a continuous layer as part of the conductor tracks, as is often the case with titanium. Such a layer of titanium is then coated with a readily conductive layer of, for example, gold, and, if necessary, a barrier layer of, for example, platinum may be interposed between the titanium and such a gold layer.

CLAIMS

1. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled, *via* a diode, to the collector of the bipolar transistor, the signal input comprising current supply means and the integrated circuit comprising a semiconductor body having a major surface adjoined by several surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first, each of the said surface regions being surrounded at the major surface by an isolation zone by means of which the surface regions are isolated electrically from each other at least during operation, One of the said surface regions of the first conductive type serves as a collector region of the bipolar transistor, said bipolar transistor furthermore has an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and is separated from the collector region in the semiconductor body by a base zone of the second conductivity type extending up to the major surface, which base zone is situated above a portion of the collector region and forms a first *p-n* junction with the said emitter zone and a second *p-n* junction with the collector region, an electrically insulating layer being present on the major surface and having a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and third apertures which are situated beside the base zone and above the collector region, the insulating layer separating from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures, each of the conductor tracks which extends into a third aperture is coupled to the collector region *via* a rectifying junction which adjoins the collector region, characterized in that an additional measure has been taken in the semiconductor structure of the bipolar transistor as a result of which a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone and collector region of said bipolar transistor so that a complementary auxiliary transistor is incorporated which has the said base zone of the second conductivity type as emitter, has the collector region of the first conductivity type as base and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

2. An integrated logic circuit as claimed in Claim 1, in which the collector region of the first conductivity type has a high-ohmic part and a low-ohmic part, the low-ohmic part extends at and along the interface with the substrate region, and the extent of the low-ohmic part of the said collector region in a direction substantially parallel to the major surface is restricted so that said low-ohmic part extends below the said emitter zone and below the said rectifying junctions but does not extend below part of said base zone underlying the second aperture in the insulating layer whereby a region of the said high-ohmic part of the collector region directly adjoins the substrate region to form a third *p-n* junction, the part of the substrate region adjoining the high-ohmic part of the collector region co-operating as a collector of the auxiliary transistor with the adjoining collector region and base zone of the bipolar transistor.

3. An integrated logic circuit as claimed in Claim 2, in which the thickness of the said high-ohmic part of the collector region measured between the second and the third p-n junction is at most 5 microns.

4. An integrated logic circuit as claimed in Claim 2 or Claim 3, in which the concentration of active dopant in the substrate region at the boundary with the high-ohmic part of the collector region of the first conductivity type is at least a factor of 10 lower than the concentration of active dopant in the low-ohmic part of the said collector region.

5. An integrated logic circuit as claimed in any of Claims 2, 3 or 4, in which the base zone of the second conductivity type has an active part which surrounds the emitter zone of the first conductivity type and an adjoining non-active part which serves for the electrical connection of the base zone and above which a second aperture is present, and said adjoining non-active part provides the emitter of the auxiliary transistor and is at least equally large as the said active part.

6. An integrated logic circuit as claimed in any of Claims 2, 3 or 4, in which the base zone of the second conductivity type has an active part which surrounds the emitter zone of the first conductivity type and an adjoining non-active part which serves for the electrical connection of the base zone and above which a second aperture is present, said non-active part provides the emitter of the auxiliary transistor, and the said second aperture has a width which is larger than the width of each of the third apertures above the collector region of the first conductivity type.

7. An integrated logic circuit as claimed in

collector region of the inverter.

The coupling diodes 16 may be obtained by means of materials other than the said platinel silicide; thus for example, aluminium, platinum silicide or titanium may be used. This material may be present only in the apertures in the insulating layer, as with the described platinel silicide junctions, or may form a continuous layer as part of the conductor tracks, as is often the case with titanium. Such a layer of titanium is then coated with a readily conductive layer of, for example, gold, and, if necessary, a barrier layer of, for example, platinum may be interposed between the titanium and such a gold layer.

CLAIMS

1. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled, *via* a diode, to the collector of the bipolar transistor, the signal input comprising current supply means and the integrated circuit comprising a semiconductor body having a major surface adjoined by several surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first, each of the said surface regions being surrounded at the major surface by an isolation zone by means of which the surface regions are isolated electrically from each other at least during operation. One of the said surface regions of the first conductive type serves as a collector region of the bipolar transistor, said bipolar transistor furthermore has an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and is separated from the collector region in the semiconductor body by a base zone of the second conductivity type extending up to the major surface, which base zone is situated above a portion of the collector region and forms a first *p-n* junction with the said emitter zone and a second *p-n* junction with the collector region, an electrically insulating layer being present on the major surface and having a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and third apertures which are situated beside the base zone and above the collector region, the insulating layer separating from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures, each of the conductor tracks which extends into a third aperture is coupled to the collector region *via* a rectifying junction which adjoins the collector region, characterized in that an additional measure has been taken in the semiconductor structure of the bipolar transistor as a result of which a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone and collector region of said bipolar transistor so that a complementary auxiliary transistor is incorporated which has the said base zone of the second conductivity type as emitter, has the collector region of the first conductivity type as base and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

2. An integrated logic circuit as claimed in Claim 1, in which the collector region of the first conductivity type has a high-ohmic part and a low-ohmic part, the low-ohmic part extends at and along the interface with the substrate region, and the extent of the low-ohmic part of the said collector region in a direction substantially parallel to the major surface is restricted so that said low-ohmic part extends below the said emitter zone and below the said rectifying junctions but does not extend below part of said base zone underlying the second aperture in the insulating layer whereby a region of the said high-ohmic part of the collector region directly adjoins the substrate region to form a third *p-n* junction, the part of the substrate region adjoining the high-ohmic part of the collector region co-operating as a collector of the auxiliary transistor with the adjoining collector region and base zone of the bipolar transistor.

3. An integrated logic circuit as claimed in Claim 2, in which the thickness of the said high-ohmic part of the collector region measured between the second and the third p-n junction is at most 5 microns.

4. An integrated logic circuit as claimed in Claim 2 or Claim 3, in which the concentration of active dopant in the substrate region at the boundary with the high-ohmic part of the collector region of the first conductivity type is at least a factor of 10 lower than the concentration of active dopant in the low-ohmic part of the said collector region.

5. An integrated logic circuit as claimed in any of Claims 2, 3 or 4, in which the base zone of the second conductivity type has an active part which surrounds the emitter zone of the first conductivity type and an adjoining non-active part which serves for the electrical connection of the base zone and above which a second aperture is present, and said adjoining non-active part provides the emitter of the auxiliary transistor and is at least equally large as the said active part.

6. An integrated logic circuit as claimed in any of Claims 2, 3 or 4, in which the base zone of the second conductivity type has an active part which surrounds the emitter zone of the first conductivity type and an adjoining non-active part which serves for the electrical connection of the base zone and above which a second aperture is present, said non-active part provides the emitter of the auxiliary transistor, and the said second aperture has a width which is larger than the width of each of the third apertures above the collector region of the first conductivity type.

7. An integrated logic circuit as claimed in

Claim 6, in which the width of the second aperture is at least twice as large as the width of each of the third apertures.

8. An integrated logic circuit as claimed in any of Claims 2 to 7, in which, as viewed on the major surface, the first, second and third apertures are arranged in a row, at least a first aperture situated above an emitter zone of the first conductivity type is present between one or more third apertures on the one hand and a second aperture on the other hand which is situated above a part of the base zone of the second conductivity type providing the emitter of the auxilary transistor.

9. An integrated logic circuit as claimed in any of the preceding Claims, in which a further surface zone of the second conductivity type adjoining the collector region of the first conductivity type is present at the major surface and beside the base zone and extends into the semiconductor body from the major surface down to substantially the same depth as the base zone, said further surface zone serving as a collector of the auxiliary transistor and being connected to the substrate region.

10. An integrated logic circuit as claimed in Claim 9, in which the distance at the major surface between the base zone and the further surface zone is at most 5 microns.

11. An integrated logic circuit as claimed in Claim 9 or Claim 10, in which the isolation zones are surface zones of the second conductivity type which extend into the semiconductor body from the major surface down to a larger depth than the said further surface zone, and the said further surface zone overlaps at the major surface the isolation zone adjoining the collector region of the first conductivity type so as to be connected directly to said isolation zone.

12. An integrated logic circuit as claimed in any of Claims 9, 10 or 11, in which the base zone of the second conductive type is surrounded at the major surface only partly by the said further surface zone, and the periphery of the said base zone at the major surface is situated partly opposite to one or more third apertures and for the whole remaining part is situated opposite to the said further surface zone.

13. An integrated logic circuit as claimed in Claim 12, in which the base zone of the second conductivity type is substantially rectangular, the said further surface zone is substantially in the form of a U and surrounds the said base zone on three sides, and the third apertures in the insulating layer are arranged besides the fourth side of said base zone.

14. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled via a diode to a collector of the bipolar transistor, which transistor has an emitter zone of a first conductivity type and a base zone of a second conductivity type opposite to the first, the signal input comprising current supply means, the integrated circuit comprising in a semiconductor body a semiconductor region of the first conductivity type which belongs to a collector region of the bipolar transistor and is situated on a substrate region of the second conductivity type, the base zone being situated above a portion of the collector region, characterized in that an additional measure has been taken in the semiconductor structure of the bipolar transistor as a result of which a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone and collector region of said bipolar transistor so that a complementary auxiliary transistor is incorporated which has the said base zone of the second conductivity type as emitter, has the collector region of the first conductivity type as base and has the said region of the second conductivity type as a convector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

15. An integrated logic circuit as claimed in Claim 14, in which the collector region of the first conductivity type has a high-ohmic part and a low-ohmic part, the low-ohmic part extends along the interface with the subsrate region so as to be present below the said emitter zone and below the part of the collector region where coupled to the signal-output diodes, but the said low ohmic part does not extend below part of the said base zone where contact by a conductor track whereby a region of the said high-ohmic part of the collector region underlying said contacted part of said base zone directly adjoins the substrate region to form a *p-n* junction therewith, which junction eactrs as a base-collector junction of the auxiliary transistor.

16. An integrated logic circuit as claimed in Claim 14 or Claim 15, in which a further surface zone of the second conductivity type is present beside the base zone of the second conductivity type, extends from the same semiconductor surface to substantially the same depth as the said base zone, and is separated from said base zone by an intermediate part of said collector region of the first conductivity type, which further surface zone serves as a collector of the auxiliary transistor and is connected to the substrate region.

17. An integrated logic circuit substantially as described with reference to Figures 2 to 4 of the accompanying drawings.

18. An integrated logic circuit substantially as described with reference to Figures 5 and 6 of the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1982. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.