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(57) Abstract: A method and apparatus for managing the variable timing of internal clock signals derived from an external clock signal in order to compensate for uncertainty and variations in the amount of read clock back timing relative to data flow to achieve and specified read latency. A reter signal is generated at DRAM initialization and starts an first counter, which counts external clock cycles, and is also passed through the slave delay line of the delay lock loop to start a second counter. The counters run continuously once started and the difference in count values represent the internal delay as an external clock signal. An internal read latency value is used to offset either counter to account for the internal read latency of the DRAM circuit. Once the non-offset counter is equivalent to the offset counter, read data is placed on an output line with a specified read latency and synchronized with the external read clock.