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COMPLETE SPECIFICATION

Amplifier

We, RADIO CORPORATION OF AMERICA, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical apparatus and in particular to electronic amplifier arrangements.

Electronic amplifiers are of fundamental importance in electronic systems. Sometimes this is apparent, as in a radio receiver, where the objective is to amplify a weak signal. Sometimes, the need for amplification is not as obvious as in an electronic computer where very few of the circuits are labeled "amplifier". However, amplification is present and important to insure against loss of signal information.

In the interest of reduced size, weight, power dissipation and cost, it is desirable to fabricate electrical amplifier circuits as integrated circuit structures. Insulated-gate field-effect transistors are particularly suitable for fabrication in integrated circuit arrangements.

An object of this invention is to provide a new and improved amplifying arrangement which includes means for connecting a bias voltage source to at least one transistor in order to operate this transistor in enhancement mode.

According to the invention, there is provided an amplifier which, in the absence of feedback, has a d.c. transfer characteristic with two low gain regions separated by a high gain region; said amplifier including one or more first insulated-gate field-effect transistors

each of which has a gate electrode connected in circuit with the input terminal of said amplifier, a load impedance connected in common to the output terminal of said amplifier and the source-drain conduction path of one of said first transistors for providing a load for this field-effect transistor, a feedback circuit coupled between said input and output terminals and including the source-drain conduction path of a second insulated gate field effect transistor, the source drain conductor path forming a d.c. path to hold the d.c. voltage at said input terminal substantially equal to the d.c. voltage at said output terminal in order to make the feedback characteristic intersect the amplifier transfer characteristic in said high gain region, and means for connecting a bias voltage source to each of said first field effect transistors by way of said load impedance in order to operate the said first transistor which has a source-drain conduction path connected in common with the load impedance and the output terminal in enhancement mode.

In the accompanying drawings:—

FIGURES 1 and 9 are circuit diagrams of stabilized amplifiers embodying the principles of the present invention;

FIGURES 2 and 10 are graphical representations of the input and output transfer characteristics of the amplifiers of FIGURES 1 and 9, respectively;

FIGURES 3 and 6 are waveform diagrams of the electrical signals occurring at various points in the amplifiers of FIGURES 1 and 9;

FIGURE 7 is a circuit diagram of another embodiment of the invention; and

FIGURE 8 is a block diagram of a plurality of amplifiers connected in cascade.

The active devices contemplated for use in practicing the invention are of a type known

in the art as insulated-gate field-effect transistors. An insulated-gate field-effect transistor may generally be defined as a majority carrier field-effect device, which includes a body of semiconductive material. A carrier conduction channel within the semiconductive body is bounded at one end thereof by a source region and at the other end by a drain region. A gate or control electrode overlies at least a portion of the carrier conduction channel and is separated therefrom by a region of insulating material. Due to the insulation between the gate electrode and the channel, the input impedance of an insulated-gate field-effect transistor is very large, on the order of 10^{15} ohms or more, so that substantially no current flows in the gate electrode circuit. Thus, the insulated-gate field-effect transistor is a voltage controlled device. Signals or voltages applied to the gate electrode control, by field-effect, the conductance, of the channel.

Two known types of insulated-gate field-effect transistors are the thin-film transistor (TFT) and the metal-oxide semiconductor (MOS). Some of the physical and operating characteristics of a thin-film transistor are described in an article, by P. K. Weimer, entitled, "The TFT—A New Thin-Film Transistor", appearing at pages 1462—1469 of the June, 1962, issue of the PROCEEDINGS OF THE IRE. The MOS transistor is described in an article entitled, "The silicon Insulated-Gate Field-Effect Transistor", by S.R. Hofstein and F.P. Heiman, appearing at pages 1190—1202 of the September, 1963, issue of the PROCEEDINGS OF THE IEEE.

Such transistors may be of either the enhancement type or the depletion type. The enhancement type unit is of particular interest in the present application. In an enhancement type unit, the impedance of the conduction channel is very high when the gate and source voltage have the same value. A signal of the proper polarity applied between the gate and source decreases the impedance of the conduction channel. In a depletion type unit, the impedance of the conduction path is relatively low when the source and gate have the same voltage. Input signals of the proper polarity applied between the source and drain increase the impedance of the conduction path.

It should be noted, however, that a depletion type transistor can be biased so that it operates as an enhancement type transistor. For example, a voltage source having an appropriate value and polarity connected in series with the gate electrode of a depletion type transistor can bias the transistor so that the impedance of its conductive channel is normally high. Input voltages of the proper polarity applied between the source electrode and the side of the voltage source remote from the gate electrode decrease the impedance of the conduction channel as in the enhancement

type transistor. The terminology, enhancement type field-effect means or device, as used in the following description and appended claims, is intended to include not only an enhancement type transistor but also a depletion type transistor which is biased to operate like an enhancement type.

An insulated-gate field-effect transistor may be either a P-type or an N-type unit depending upon the majority carriers involved in drain current conduction. A P-type unit is one in which the majority carriers are holes; whereas, an N-type unit is one in which the majority carriers are electrons.

Referring now to FIGURES 1 and 9 in which like reference characters denote similar components, the amplifier of the present invention is illustrated in two embodiments of similar circuit construction. In each embodiment the amplifier has an input connection 4 which is connected to the gate electrode 1g of an N-type insulated-gate field-effect transistor 1. The drain electrode 1d of the transistor 1 is connected to the amplifier output connection 5.

A load impedance, illustrated as the conduction path of an insulated-gate field-effect transistor 2, is also connected to the output connection 5. In FIGURE 1, the transistor 2 is a P-type having its drain electrode 2d connected to the output connection 5, its source electrode 2s connected to an electrical connection 16, and its gate electrode 2g connected to the input connection 4. In FIGURE 9, the transistor 2 is an N-type having its source electrode 2s connected to the output connection 5 and both its gate electrode 2g and drain electrode 2d connected to the electrical connection 16.

A feedback path between the amplifier input and output connections 4 and 5 includes a feedback impedance illustrated as an insulated-gate field-effect transistor 3 of the P-type in FIGURE 1 and of the N-type in FIGURE 9. To this end, the source electrode 3s is connected to the output connection 5 and the drain electrode 3d is connected to the input connection 4. The gate electrode 3g is connected to the electrical connection 18. The amplifier circuits thus far described may be fabricated as articles in integrated circuit structures or modules.

For use in an electrical circuit, the input connection 4 in either FIGURE 1 or 9 is coupled to a first terminal 7 of a signal source or generator 6. The gate electrode 3g of the feedback transistor 3 is connected to a second terminal 8 of the signal generator 6 by way of the connection 18. The signal generator 6 represents the system with which the amplifier is associated. A suitable operating voltage, illustrated as a battery V_b , has its positive terminal connected to the source electrode 2s of transistor 2 and has its negative terminal connected to a point of reference potential in-

indicated in the drawing by the conventional ground symbol. The source electrode 1s of the transistor 1 is also connected to circuit ground, as shown by the conventional symbol in FIGURES 1 and 9.

D.C. Operating Conditions

The d.c. transfer characteristics for the amplifiers of FIGURES 1 and 9 are illustrated in FIGURES 2 and 10, respectively, by plots of the electrical output signal e_o versus the input signal e_i . The transfer characteristics in both FIGURES 2 and 10 have a high gain region 10 and boundary or low gain regions regions 11 and 12. Each of the signals e_i , e_o , and e_o is considered to have a static d.c. component and a dynamic component. For the purpose of considering the d.c. operating characteristics of the amplifiers, the dynamic components are assumed equal to zero.

Referring first to the amplifier of FIGURE 1 and the plot of FIGURE 2, it is assumed at the outset that the feedback transistor 3 is not connected between the input and output connections 4 and 5. When the d.c. component of the input signal e_i is at or near zero e_i is at or near zero volt, the gate-to-source voltage of P-type transistor 2 is substantially $-V_b$ volt, and the gate-to-source voltage of the N-type transistor 1 is at substantially zero volt. Thus, the P-type transistor 2 is biased to a fully conductive condition and the transistor 1 is biased into cut-off. The d.c. component of the output signal e_o has substantially the value of the operating voltage V_b , since the impedance of the channel of the P-type transistor 2 is nearly zero and the impedance of the channel of the N-type transistor is nearly infinite. For these conditions, the amplifier is operating in the low gain region 11 of its transfer characteristic.

As the input signal e_i increases, the gate-to-source voltage of the P-type transistor increases in a positive direction, thereby tending to decrease the conductance of its channel. The gate-to-source voltage of the N-type transistor also increases positively as the input signal e_i exceeds the threshold V_{TN} of the N-type transistor 1. Thus, as the input signal e_i increases, the N-type transistor 1 becomes conductive and both transistors 1 and 2 are conducting. For these conditions, the amplifier operates in the high gain region 10 of its transfer characteristic and the output signal e_o has a d.c. value which is less than V_b .

As the input signal e_i becomes more positive, the gate-to-source voltage of the P-type transistor approaches the threshold V_{TP} of the P-type transistor 12, thereby tending to bias the P-type transistor into cut-off. The gate-to-source voltage of the N-type transistor increases in the positive direction, thereby tending to bias the N-type transistor into a fully conducting condition. The output signal

e_o decreases and approaches a value of substantially zero volt. For these conditions, the amplifier operates in the low gain region 12 of its transfer characteristic. To summarize, the amplifier operates in the high gain region 10 when both transistors 1 and 2 are conducting and operates in the low gain regions 11 and 12 when only one of the transistors 1 and 2 is conducting.

The feedback transistor 3 stabilizes the amplifier in the high gain region 10 of its transfer characteristic. Again consider that the dynamic components of the electrical signals e_i , e_o , and e_o are zero. Assume also that the static d.c. component of the electrical signal e_i is zero volts so that the P-type transistor 3 is conducting. For these conditions, the static d.c. components of the signal e_o and e_i become equal to one another. Both P-type transistors 2 and 3 and the N-type transistor 1 are biased into conductive regions of their operating characteristics. The 45° line 13 in FIGURE 2 represents the $e_o = e_i$ characteristic. The intersection 14 of the line 13 with the high gain region 10 of the amplifier transfer characteristic represents the d.c. operating point on the amplifier.

It is convenient to describe this d.c. stabilization in terms of the input and output capacitances C_{in} and C_o . The capacitance C_{in} is the capacitance seen looking into the amplifier between the input connection 4 and ground; whereas the output capacitance C_o is the capacitance seen looking back into the amplifier between the output connection 5 and ground. These capacitances include the interelectrode, substrate and other stray capacitance.

Assuming that the output impedance of the signal generator 6 is infinite, the input capacitance C_{in} and the output capacitance C_o become charged to the same d.c. voltage so that no current is conducted by the channel of the P-type transistor 3. For the case where the output impedance of the signal generator is finite, a coupling capacitor C_c is necessary to maintain the charge of the input capacitance C_{in} .

The previous assumption that the static d.c. component of the electrical signal e_i is zero is made for the purposes of illustration. This static d.c. component could have any appropriate value relative to the operating voltage V_b so long as all of the transistors 1, 2 and 3 are biased into conduction. It should be noted that the transistor 3 may be an N-type as in FIGURE 9 instead of a P-type in which case the d.c. component of e_i must have an appropriate value to bias the transistor 2 into conduction.

The amplifier always stabilizes at $e_o = e_i$ in the high gain region 10 regardless of differences in the characteristic of the P and N-type transistors. That is to say, the 45° line 13 always intersects the d.c. transfer

characteristic in the high gain region 10, whether or not the characteristics of the P and N-type transistors 1 and 2 are symmetrical.

5 Although the conduction path of transistor 2 has been previously described as a load impedance for transistor 1, it is apparent that the conduction path of transistor 1 is also a load impedance for transistor 2 in the amplifier of FIGURE 1 due to the symmetry of the circuit. This is not true, however, for the amplifier of FIGURE 9. In FIGURE 9, the primary function of transistor 2 is to provide a load impedance for transistor 1. This may be accomplished by making transistor 1 much larger physically than transistor 2. Thus, the impedance of the conduction path of transistor 2 will be substantially higher than the conduction path of transistor 1. Due to the connection of the gate electrode 2g to the drain electrode 2d, the N-type transistor 2 is continually biased into conduction. The level or amount of conduction, however, depends upon the d.c. conditions at the source electrode 2s and, hence, the output connection 5.

The plot in FIGURE 10 of the amplifier d.c. transfer characteristic of the circuit of FIGURE 9 illustrates these conditions both and without the feedback transistor 3. First consider that feedback transistor 3 is not in the circuit. Also consider that transistor 1 and 2 have threshold voltages V_{T1} and V_{T2} , respectively. When the d.c. component of the input signal e_1 is less than V_{T1} volts, the transistor 1 is turned off so that the impedance of its channel is relatively high. The impedance of the channel of the conducting transistor 2 is much lower whereby the output capacitance C_o is charged to a voltage of $V_b - V_{T2}$. Thus, the transistor 2 is just barely conducting to maintain the voltage across C_o . For these conditions, the amplifier is operating in the low gain region 11 of its transfer characteristic.

As the d.c. component of the input signal e_1 becomes more positive than V_{T1} , the N-type transistor 1 is conducting whereby the impedance of its conduction path becomes smaller. The output voltage e_o or the voltage across the capacitance C_o now has a value dependent upon the voltage divider action of the conduction path impedances of the transistors 1 and 2. For this condition, the amplifier is operating in the high gain region 10 of its transfer characteristic.

As the d.c. component of the input signal e_1 becomes more positive, the transistor 1 becomes more conductive whereby the impedance of its conduction path becomes smaller. As the conduction path impedance of transistor 1 decreases, the output signal e_o decreases and approaches a value of substantially 0 volt. When the output signal e_o has a value of 0 volt, both transistor 1 and transistor 2 are fully conductive and substantially all of the

voltage V_b is dropped across the conductive path of the transistor 2. This is due to the higher impedance of the conductive path of transistor 2 as compared to the conductive path of transistor 1. For these conditions, the amplifier operates in the low gain region 12 of its transfer characteristic.

As in the embodiment of FIGURE 1, the feedback transistor 3 also serves to stabilize the amplifier of FIGURE 9 at the point 14 in the high gain region 10 of the transfer characteristic as shown in FIGURE 10. The d.c. component of the signal e_2 is positive enough to bias N-type transistors 3 into conduction. The static d.c. components of the signals e_1 and e_o becomes equal so that the amplifier is d.c. stabilized at the intersection 14 of the d.c. feedback characteristic curve 13 with the high gain region 10 of the amplifier d.c. transfer characteristic.

Although the amplifier embodiment of FIGURE 9 has been illustrated with all N-type transistors it is apparent that all P-type transistors can be used so long as the appropriate voltage values are changed. Further it is apparent that the only requirement for the feedback transistor 3 is that it be d.c. biased into conduction so that its conductivity type has substantially no effect on the stabilization of the amplifier. Thus a P-type feedback transistor 3 can be used with N-type transistors 1 and 2 and vice versa.

The amplifier embodiment of FIGURE 9 is especially attractive for linear amplification because the absolute value of gain is dependent only on the ratio of the linear dimensions of the transistors 1 and 2. Both of the amplifier embodiments as illustrated are especially suited for integrated circuit structures since each is comprised only of active transistor devices. However, it should be noted that the principles embodied in the illustrations of FIGURES 1 and 9 are fully applicable to the case where either or both of the load and feedback impedances are passive devices.

Dynamic Operation

For a given frequency of the dynamic component of the signal e_1 , the amplifier embodiments of FIGURES 1 and 9 have either a constant or a variable gain depending upon the electrical signal e_2 applied at the gate electrode 3g of the transistor 3. If the dynamic component of the signal e_2 is zero, its d.c. component maintains the impedance of the channel between the source 3s and the drain 3d constant. So long as this impedance remains constant, the gain of the amplifier remains constant.

On the other hand, if the dynamic component of the signal e_2 varies as a function of time, the impedance of the channel between the source 3s and the drain 3d also varies. In other words, the conduction channel of the feedback transistor 3 is an impedance;

and the gate 3g is a voltage control means which controls the value of the impedance.

The gain G_f of any amplifier with feedback is given by

$$G_f = \frac{G_o}{1 + \beta G_o}$$

where G_o is the gain without feedback and β is the amount of output signal fed back to the input. Variations of the impedance of the channel of the feedback transistor 3 results in variations of the amount of output signal fed back to the input and, therefore, variations in β . Consequently, the amplifier embodiments of FIGURES 1 and 9 operate as constant gain amplifiers for the case where no dynamic signal is applied to the gate 3g and as variable gain amplifiers for the case where a dynamic signal is applied to the gate 3g.

During a particular time period, the dynamic components of the electrical signals e_1 and e_2 may be analog or continuous in nature or they may be intermittent in nature occurring only during discrete intervals within the time period. In the following description, illustrations are given for the cases (1) where both signals e_1 and e_2 are continuous functions of time; (2) where e_1 is intermittent, and e_2 is continuous; (3) where e_1 is continuous, and e_2 is intermittent; and (4) where both e_1 and e_2 are intermittent.

Case I

The case where both electrical signals e_1 and e_2 are analog or continuous in nature during the time period under consideration is shown in FIGURE 3. For ease of illustration, both signals e_1 and e_2 are shown to be periodic signals each having a single frequency component. The electrical signal e_2 has a d.c. component edc_2 as illustrated by waveform (b) in FIGURE 3. Where the frequency of the signal e_1 is higher than the frequency of the signal e_2 , the amplifier operates as a modulator. Thus, the waveform (a) is the carrier signal e_1 ; the waveform (b) is the modulating signal e_2 ; and the waveform (c) is the modulated output signal e_o . A typical application for this modulator is in a radio transmitter type apparatus. For such an application the signal e_2 is an audio signal having a plurality of audio frequency components and the signal e_1 is the r.f. carrier.

According to the previous description of the static d.c. operation, the d.c. components of the carrier signal e_1 and the modulator output signal e_o are identical. In addition, the single stage amplifier embodiments illustrated in FIGURES 1 and 9 are inverting type amplifiers, as can be seen by the inverted modulated carrier in FIGURE 3(c).

Case II

The case where the signal e_1 is intermittent and where the signal e_2 is continuous during the time period under consideration is illustrated in FIGURE 4. Again for ease of illustration, the signal e_2 is shown as a single frequency sinusoid in waveform (b) having a d.c. component edc_2 . The signal e_1 is shown in waveform (a) as a pulse train having a rate of occurrence greater than the frequency of the signal e_2 . Again, the amplifier is operative as a modulator and provides a pulse modulator output signal e_o , as shown in waveform (c). A typical application is in communications type apparatus wherein the signal e_2 is generally a multi-frequency information signal and the signal e_1 is the carrier signal.

Case III

The case where the signal e_1 is analog or continuous and where the signal e_2 is intermittent during the time period under consideration is illustrated in FIGURE 5. Again, for convenience of illustration, the signal e_1 is illustrated as a single frequency sinusoid in waveform (a). The signal e_2 is illustrated in waveform (b) as a pulse which occurs only during a discrete interval or intervals during the time period under consideration. The polarity of this pulse as illustrated is for use with a P-type transistor 3 as illustrated in FIGURE 1. For use with an N-type transistor 2 as in FIGURE 9, the pulse polarity should be reversed.

Prior to the occurrence at time t_1 of the leading edge of the pulse signal e_2 , the amplifier is operative with a constant gain to amplify the input signal e_1 . When the pulse signal e_2 is applied to the gate 3g of the feedback transistor from time t_1 to time t_2 , the impedance of the feedback channel increases so that less output signal is fed back to the input. The gain of the amplifier increases with the result that from time t_1 to time t_2 the output signal e_o is much larger than either before time t_1 or after time t_2 .

A typical application is a gate or strobe amplifier where the output signal e_o is being applied to a threshold device. In such an application the threshold device would be responsive only to the increased amplitude of the output signal e_o during the presence of the gating pulse e_2 .

Case IV

The case where both signals e_1 and e_2 occur only at discrete intervals during the time period under consideration is illustrated in FIGURE 6. This case is similar to the CASE III in that the signal e_2 increases the gain of the amplifier during a gating or strobing interval. Again the illustrated polarity of the e_2 pulse is for a P-type transistor 3. For an N-type transistor 3, the pulse polarity should be reversed. Although the signal e_1 is

illustrated in waveform (a) as a square pulse, it may be of any shape so long as it occurs only during the discrete interval defined by times t_1 and t_2 . The signal e_2 increases the gain of the amplifier for the interval t_1 to t_2 so that output signal e_0 occurring during this interval is a product of the increased gain.

A typical application is as a sense amplifier for a computer memory wherein the signal e_1 is the signal being sensed and the signal e_2 is a clock signal. It should be apparent to those skilled in the art that the clock signal e_2 need not overlap the sense signal e_1 but may be present only during a portion of the time duration of the sense signal.

The circuit in FIGURE 7 illustrates the connection of a pair of opposite conductivity type feedback transistors 3 and 9 between the input and output connections 4 and 5, respectively. Circuit components in FIGURE 7 which are the same as corresponding components in FIGURE 1 are designated by the same reference characters. The additional feedback transistor 9 is an N-type having its conduction channel connected in parallel with the conduction channel of the feedback transistor 3. To this end, the drain 9d and the source 9s are connected to the input and output connections 4 and 5, respectively. Each feedback transistor 3 and 9 is illustrated by dashed connections to have gate-to-source capacitances C_3 and C_9 , respectively. An electrical signal e_3 is applied to the gate 9g of the additional feedback transistor 9.

Consider that the static or d.c. components of the signals e_2 and e_3 are such that transistors 3 and 9 both conduct. For example, assume that e_{dcs} is zero volt and that e_{dcs} is $+V_b$ volt. For the previously described CASE IV of a gating or strobing amplifier, the signal e_2 is in the form of a positive pulse 20 at the sampling interval. Due to the gate-to-source capacitance C_3 , there appear at the output connection 5, spikes 21 and 22 coincident with the leading and trailing edges of the pulse 20 and having the illustrated polarities. These spikes 21 and 22 are obviously undesirable in that they distort the amplifier signal e_1 .

The additional N-type feedback transistor 9 operates to substantially cancel the spikes 21 and 22. To this end, the signal e_3 is illustrated as a negative pulse 23 of which the leading and trailing edges are coincident with the leading and trailing edges of the pulse 20. Due to the capacitance C_9 the spikes 24 and 25, respectively, occur coincident with the leading and trailing edges of the pulse 23 and with polarities which are opposite to the polarities of the spikes 21 and 22. Consequently, the spikes 24 and 25 tend to cancel the spikes 21 and 22 so that there is substantially no distortion of the amplified

signal appearing at output terminal 5 due to the capacitances C_3 and C_9 .

It is also apparent that in an integrated circuit, the drains 1d and 2d of transistors 1 and 2 and the sources 3s and 9s of the transistors 3 and 9 could be connected by a region in the semiconductor material which is common to the conduction channel of each of the four transistors. It is further apparent that in integrated form the gates 1g and 2g could be a single gate electrode which is insulated from and common to the conduction channel of each of the transistors 1 and 2.

The amplifier embodiments of FIGURES 1 and 9 are inverting types which may be considered as single stage amplifiers. In these embodiments, the feedback transistor 3 functions to provide d.c. stabilization in the high gain regions of the transfer characteristics. If an odd plurality of insulated-gate transistor inverting amplifier stages are connected in cascade, a single feedback impedance or insulated-gate field-effect transistor connected between the output and input can provide not only d.c. stabilization but also can prevent the amplifier from oscillating and thus provide a.c. stabilization.

In FIGURE 8, a plurality n of inverting type insulated-gate field-effect transistor amplifier stages $A_1, A_2, \dots, A_n$ are coupled in cascade by way of coupling links $CL_1, CL_2, \dots, CL_{n-1}$. The coupling links may include a strictly conductive connection from the output of one stage to the input of the next stage without disturbance of the static d.c. operating voltage so long as the output impedance of the signal generator 6 is infinite or a coupling capacitor C_0 is connected between signal generator terminal 7 and the input connection 4₁ of the first amplifier stage A_1 . The amplifier stages $A_1, A_2, \dots, A_n$ may or may not have the feedback transistor 3 coupled between their respective input and output connections 4 and 5. For the case where the feedback transistor 3 is so connected in each amplifier stage, the gate electrodes 3_{g1}, 3_{g2}, $\dots$, 3_{gn} are illustrated as connected to the terminal 8 of the signal generator 6. The output connection 5_n of the last stage A_n is connected by way of a feedback circuit 15 to the input connection 4₁ of the first amplifier stage A_1 .

As mentioned previously, where n is an odd number, the cascaded amplifier can be stabilized by means of a single feedback impedance. Thus, the feedback circuit 15 may include an impedance, such as the conduction path of an insulated-gate field-effect transistor, connected between the output 5_n and the input 4₁. Although each amplifier stage may include a feedback transistor 3 which is biased into conduction, the feedback transistors 3 are not necessary and may either be eliminated or biased into nonconduction by way of signal generator terminal 8. The feed-

back impedance 15 therefore serves to d.c. stabilize the entire amplifier even where the coupling links CL are direct connections and to a.c. stabilize the amplifier with appropriate negative feedback over the frequency range of interest.

The cascaded amplifier embodiment of FIGURE 8 can function with constant or with variable gain. For constant gain operation the feedback impedance 15 is held constant. Variable gain is achieved by providing one or more of the stages $A_1, A_2, \dots, A_n$ with feedback transistors 3 and applying control signals to the gate electrodes thereof. For example, the first stage A_1 may be provided with a feedback transistor 3 and the control signal e_2 (FIGURE 1 or FIGURE 9) may be applied thereto. The remainder of the amplifier stages $A_2 \dots A_n$, which need not have feedback transistors, function to amplify the output signal provided by the first stage.

When the FIGURE 8 amplifier is operated with constant gain, the feedback circuit 15 may also include any conventional network to achieve the typical operational functions.

The amplifier embodiments of FIGURES 1, 7, 8 and 9 are especially attractive for use in integrated circuit structures since all components including feedback impedance 15 (FIGURE 8) can be insulated-gate field-effect transistors. The preceding description of the dynamic operation of the amplifier is based on the assumption that the dynamic signal e_1 is a small signal so that the amplifier operates solely within its linear range or the region 10 in FIGURES 2 and 10. However, this is not necessary. The dynamic signal e_1 may be large enough so that either the transistor 1 or the transistor 2 (in the case of FIGURE 1) becomes cut off due to application of this signal. This corresponds to operation in both region 10 and one of the regions 11 or 12 in FIGURES 2 and 10.

Reference is hereby made to our copending application No. 14632/69 Serial No. 1163942 relating to and claiming an amplifier.

WHAT WE CLAIM IS:—

1. An amplifier which, in the absence of feedback, has a d.c. transfer characteristic with two low gain regions separated by a high gain region; said amplifier including one or more first insulated gate field effect transistors each of which has a gate electrode connected in circuit with the input terminal of said amplifier, a load impedance connected in common to the output terminal of said amplifier and the source-drain conduction path of one of said first transistors for providing a load for this field effect transistor, a feedback circuit coupled between said input and output terminals and including the source-drain conduction path of a second insulated gate field effect transistor, the source drain conduction path forming a d.c. path to hold

the d.c. voltage at said input terminal substantially equal to the d.c. voltage at said output terminal in order to make the feedback characteristic intersect the amplifier transfer characteristic in said high gain region, and means for connecting a bias voltage source to each of said first field effect transistors by way of said load impedance in order to operate the said first transistor which has a source-drain conduction path connected in common with the load impedance and the output terminal in enhancement mode.

2. An amplifier as defined in claim 1, wherein said load impedance is the source-drain conduction path of a third insulated gate field effect transistor.

3. An amplifier as defined in claim 2, wherein said first and third insulated gate field effect transistors are of the same conductivity type, and wherein said third transistor has its gate electrode connected to one end of its source-drain conduction path.

4. An amplifier as defined in claim 3, wherein the first transistor is physically larger than the third transistor.

5. An amplifier as defined in claim 2, wherein said first and third transistors are of opposite conductivity types, and wherein said third transistor has its gate electrode connected to said input terminal.

6. An amplifier as defined in claim 1, 2, 3, 4, or 5, wherein said amplifier is adapted to receive input signal energies independently applied to said input terminal and to the gate electrode of said second transistor.

7. An amplifier as defined in claim 6, wherein said input signal energies includes a first electrical signal applied to said input terminal and a second electrical signal applied to the gate electrode of said second transistor and in that both of said electrical signals are variable with time whereby said amplifier operates as a variable gain amplifier.

8. An amplifier as defined in claim 3, wherein the conductivity of said second transistor is the same as the conductivities of said first and third transistors.

9. An amplifier as defined in claim 1 or 2, wherein said feedback path additionally includes the source drain conduction path of a fourth insulated gate field effect transistor connected in parallel to the source drain conduction path of said second transistor, and wherein said second and fourth transistors are of opposite conductivity type.

10. An amplifier as claimed in any one of the preceding claims as an integrated circuit structure or module.

11. An amplifier wherein a plurality of amplifiers according to any one of the preceding claims are connected in cascade.

12. An amplifier as defined in claim 11, wherein the number of said amplifiers is odd and there is a feedback network connected between the output connection of the last of



back impedance 15 therefore serves to d.c. stabilize the entire amplifier even where the coupling links CL are direct connections and to a.c. stabilize the amplifier with appropriate negative feedback over the frequency range of interest.

The cascaded amplifier embodiment of FIGURE 8 can function with constant or with variable gain. For constant gain operation the feedback impedance 15 is held constant. Variable gain is achieved by providing one or more of the stages $A_1, A_2, \dots, A_n$ with feedback transistors 3 and applying control signals to the gate electrodes thereof. For example, the first stage A_1 may be provided with a feedback transistor 3 and the control signal e_2 (FIGURE 1 or FIGURE 9) may be applied thereto. The remainder of the amplifier stages $A_2, \dots, A_n$, which need not have feedback transistors, function to amplify the output signal provided by the first stage.

When the FIGURE 8 amplifier is operated with constant gain, the feedback circuit 15 may also include any conventional network to achieve the typical operational functions.

The amplifier embodiments of FIGURES 1, 7, 8 and 9 are especially attractive for use in integrated circuit structures since all components including feedback impedance 15 (FIGURE 8) can be insulated-gate field-effect transistors. The preceding description of the dynamic operation of the amplifier is based on the assumption that the dynamic signal e_1 is a small signal so that the amplifier operates solely within its linear range or the region 10 in FIGURES 2 and 10. However, this is not necessary. The dynamic signal e_1 may be large enough so that either the transistor 1 or the transistor 2 (in the case of FIGURE 1) becomes cut off due to application of this signal. This corresponds to operation in both region 10 and one of the regions 11 or 12 in FIGURES 2 and 10.

Reference is hereby made to our copending application No. 14632/69 Serial No. 1163942 relating to and claiming an amplifier.

WHAT WE CLAIM IS:—

1. An amplifier which, in the absence of feedback, has a d.c. transfer characteristic with two low gain regions separated by a high gain region; said amplifier including one or more first insulated gate field effect transistors each of which has a gate electrode connected in circuit with the input terminal of said amplifier, a load impedance connected in common to the output terminal of said amplifier and the source-drain conduction path of one of said first transistors for providing a load for this field effect transistor, a feedback circuit coupled between said input and output terminals and including the source-drain conduction path of a second insulated gate field effect transistor, the source drain conduction path forming a d.c. path to hold

the d.c. voltage at said input terminal substantially equal to the d.c. voltage at said output terminal in order to make the feedback characteristic intersect the amplifier transfer characteristic in said high gain region, and means for connecting a bias voltage source to each of said first field effect transistors by way of said load impedance in order to operate the said first transistor which has a source-drain conduction path connected in common with the load impedance and the output terminal in enhancement mode.

2. An amplifier as defined in claim 1, wherein said load impedance is the source-drain conduction path of a third insulated gate field effect transistor.

3. An amplifier as defined in claim 2, wherein said first and third insulated gate field effect transistors are of the same conductivity type, and wherein said third transistor has its gate electrode connected to one end of its source-drain conduction path.

4. An amplifier as defined in claim 3, wherein the first transistor is physically larger than the third transistor.

5. An amplifier as defined in claim 2, wherein said first and third transistors are of opposite conductivity types, and wherein said third transistor has its gate electrode connected to said input terminal.

6. An amplifier as defined in claim 1, 2, 3, 4, or 5, wherein said amplifier is adapted to receive input signal energies independently applied to said input terminal and to the gate electrode of said second transistor.

7. An amplifier as defined in claim 6, wherein said input signal energies includes a first electrical signal applied to said input terminal and a second electrical signal applied to the gate electrode of said second transistor and in that both of said electrical signals are variable with time whereby said amplifier operates as a variable gain amplifier.

8. An amplifier as defined in claim 3, wherein the conductivity of said second transistor is the same as the conductivities of said first and third transistors.

9. An amplifier as defined in claim 1 or 2, wherein said feedback path additionally includes the source drain conduction path of a fourth insulated gate field effect transistor connected in parallel to the source drain conduction path of said second transistor, and wherein said second and fourth transistors are of opposite conductivity type.

10. An amplifier as claimed in any one of the preceding claims as an integrated circuit structure or module.

11. An amplifier wherein a plurality of amplifiers according to any one of the preceding claims are connected in cascade.

12. An amplifier as defined in claim 11, wherein the number of said amplifiers is odd and there is a feedback network connected between the output connection of the last of

the cascaded amplifier stages and the input connection of the first of the cascaded amplifier stages.

5. 13. An amplifier substantially as described and illustrated with respect to Figure 1 of the accompanying drawings.

14. An amplifier substantially as described and illustrated with respect to Figure 8 of the accompanying drawings.

15. An amplifier substantially as described and illustrated with respect to Figure 9 of the accompanying drawings. 10

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