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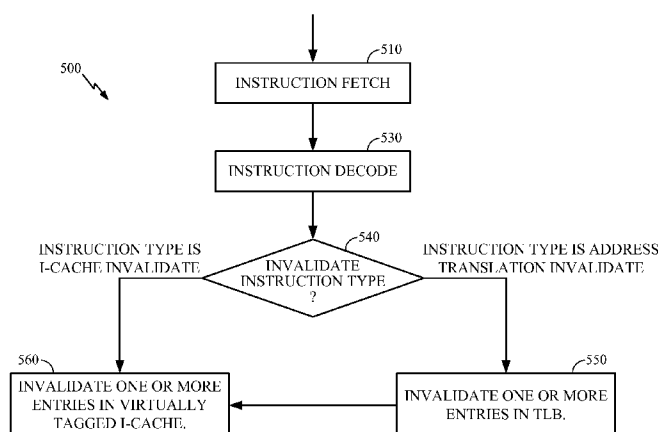
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Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: VIRTUALLY-TAGGED INSTRUCTION CACHE WITH PHYSICALLY-TAGGED BEHAVIOR



(57) Abstract: An instruction cache system having a virtually tagged instruction cache which, from a software program perspective, operates as if it were a physically tagged instruction cache is disclosed. The instruction cache system also includes a means for address translation which is responsive to an address translation invalidate instruction and a control logic circuit. The control logic circuit is configured to invalidate an entry in the virtually tagged instruction cache in response to the address translation invalidate instruction.



- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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