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A LOCOS MASK FOR SUPPRESSION OF NARROW SPACE FIELD OXIDE THINNING AND OXIDE PUNCH THROUGH EFFECT

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to processes for the manufacture of semiconductor devices and more particularly to processes for forming field isolation.

(2) Description of prior art

The formation of integrated circuit devices on silicon substrates requires that a means be provided to electrically isolate the various circuit components from each other. In many cases p/n junctions themselves can be used to form at least part of the necessary isolation. Most isolation requirements, which cannot be resolved by circuit design, relate to the lateral isolation of devices. To some extent, junction isolation can be used here also. However, as device technology leads to smaller and smaller geometries as well

as shallower structures, junction isolation technology becomes very limited.

The successful use of silicon for integrated circuits for the last thirty years can, in part, be attributed to the marvelous insulating properties of it's oxide. No other commonly known semiconductor material has this unique feature. Thus silicon oxide has become well established as the isolation material for integrated circuit chips. Earliest usage of this material involved growing it on the substrate in selected regions which are defined by an oxidation masking material. To this end, silicon nitride came into widespread use. Referring to Fig. 1, a pad silicon oxide film 22 several hundred Angstroms thick is grown on the surface of a silicon wafer 20. Next a film of silicon nitride 24 is deposited to a thickness of several thousand Angstroms using a chemical-vapor-deposition process. The pad oxide 22 is used as a buffer layer, preventing the highly stressed silicon nitride from causing dislocations in the silicon.

Using standard photolithographic techniques followed by etching, a pattern is defined in the oxide/nitride mask, leaving bare those regions 26 on the silicon which are to become isolation regions. Referring next to Fig. 2, the wafer 20 is subjected to an oxidizing ambient at elevated temperatures, during which the exposed areas are converted to silicon oxide 28. The oxidation proceeds at the oxide-silicon interface. Thereby pockets of silicon oxide 27 several thousand

Angstroms deep can be formed in the patterned areas. These pockets 27 provide the necessary electrical isolation for the subsequently formed semiconductor devices.

The process just described has become known by several names, one of which is LOCOS an acronym for LOCal Oxidation of Silicon. LOCOS has been practiced for over twenty-five years and has been adapted to many specific applications. One of the problems with conventional LOCOS, illustrated in Fig. 2 is that the pad oxide 22 permits oxidation to take place under the silicon nitride mask, pushing up the edge of the mask and thereby leaving a raised portion of the oxide around the mask perimeter, known as "Birds Head" 28 and a protrusion of oxide under the edge of the oxidation mask 29, caused by diffusion of oxidant through the thin pad oxide 22, known as "Birds Beak". The birds head 28, being a protrusion above the surface, causes shadowing and thinning problems with subsequently deposited metallization stripes traversing across it. Thin areas in metal interconnection lines constitute "weak spots" and are subject to increased current density, heating, and subsequent electrical failure. The birds beak 29 can be reduced by using as thin as possible pad oxide 22 or by stiffening the mask by using a thicker silicon nitride layer 24.

In some instances, a sidewall oxidation barrier is formed along the mask

edge to prevent penetration of the oxidant under the nitride mask. **Ema et.al. US5,453,397** describes such a barrier wherein a nitride plug is formed in a recess produced by undercutting the pad oxide with a wet etch. **Shimizu, et.al., US5,472,906** form a nitride barrier which extends over the edge of the pad oxide and over the edge of a subjacent depression in the silicon. Unfortunately, these practices lead to an abrupt feature **25** wherein high shearing stresses are produced in the silicon which lead to the formation of dislocations. These dislocations propagate diagonally into the device active regions causing junction failure.

Typically, the field oxide is grown at temperatures above 1,000°C . At these temperatures, stresses which would be developed due to the volume expansion, are relieved by plastic flow of the oxide. However, upon completion of the oxidation, and when the wafer is cooled, sufficient plastic flow is no longer able to relieve stresses below about 960°C (**Wolf, S.**,"Silicon Processing for the VLSI Era", Vol.2, Lattice Press, Sunset Beach, CA, (1990),p693). Thermal stresses now develop due to the difference in thermal expansion coefficients of the silicon oxide and the silicon. The profile of the field oxide is now the determining factor for the distribution of stresses within the silicon. Abrupt features in the silicon/silicon oxide profile, such as **25** in Fig. **2**, are responsible for high values of x-y shearing stresses which produce dislocations. Such abrupt

features **25** occur when a stiff mask edge is used to control the field oxidation.

The compressive stresses developed within the growing field oxide also have been observed to retard the oxidation rate of silicon. Known as the field oxide thinning effect, this phenomena is observed when field oxide is grown in mask openings below about 0.5 to 0.6 microns. See for example, **P. Belluti and M. Zen** in J. Electrochem. Soc. 143, (1996) p 2953.

Efforts to diffuse the abruptness of a stiff mask edge and to control the extent of birds beak encroachment into the silicon active area as well as the shape of the birds head, have been made using "L" shaped spacers which form a foot at the mask edge. **Jang US5,397,733** describes several embodiments by which these spacers can be formed. An example of the use of such a spacer is shown in Fig. **3**. The nitride foot **30** surrounding the periphery of the thicker nitride mask provides a region of more flexible mask at the edge of the opening, thereby allowing easier expansion of the growing field oxide under it. The thicker, and therefore stiffer, section **32** continues to constrict the birds beak.

By proper selection of the thickness and length of the mask foot **30** as well as the thickness of the more rigid portion **32** , it becomes possible to tailor the mask edge to provide a field oxide profile **36** with reduced stress at the

expense of minimal birds beak encroachment. **Jang** cites prior art difficulties in forming the L-shaped spacer, specifically, difficulties in controlling thickness and length of the spacer.

In one embodiment cited by **Jang** a nitride foot is formed by first depositing a silicon nitride layer over a pad oxide, thinning a region of the nitride layer to form a step, depositing a polysilicon layer over the step, and applying a spacer etch which forms a polysilicon spacer at the edge of the region. The nitride layer is then etched into the pad oxide using the polysilicon spacer to protect the nitride foot. The polysilicon spacer is subsequently removed from over the foot, permitting the foot to flex during the field oxidation.

The precise tailoring of the field oxidation mask edge becomes even more critical as device geometries shrink into the sub-half micron range. As field oxide widths approach these dimensions oxidation rates are significantly retarded and stress induced crystalline defects cause serious degradation of the semiconductor devices. The balance between reducing birds beak encroachment and preventing stress induced dislocations requires an even greater control of the field oxide oxidation mask edge. The invention herein described provides a foot with a continuous transition of flexibility from its tip to the main portion of the mask. The risk of cracking at the foot/mask interface is

also reduced. In addition, the invention eliminates process steps required by **Jang** for spacer removal to provide a flexible foot for the field oxidation.

Chiu et.al., US5,470,783 shows the formation of a nitride foot at the base of the main nitride oxidation mask used for the formation of recessed oxide isolation. The foot is not tapered and functions to reduce the oxidation window of the opening, thereby reducing penetration of the recessed oxide under the main portion of the mask.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a method for forming a field oxide isolation compatible with sub-half-micron device technology having reduced stress induced dislocations.

It is another object of this invention to provide a method for forming a field oxide isolation having a smooth surface topology at its periphery, thereby improving step coverage of subsequently deposited conductive layers.

It is yet another object of this invention to provide a method for forming a field oxide isolation with improved minimal birds beak encroachment into device active areas.

It is still another object of this invention to provide a method for suppressing the field oxide thinning effect which occurs when field oxide is grown between narrow mask spacings.

It is still another object of this invention to provide a method for suppressing the oxide punch through effect which occurs when field oxide is grown between narrow mask spacings.

It is yet another object of this invention to describe a novel oxidation mask which will yield an improved field oxide isolation for use with sub half-micron integrated circuit technology.

It is still another object of this invention to provide a method for forming an oxidation mask having a flexible foot with reduced risk of cracking of the foot at its junction with the main portion of the oxidation mask.

These objects are accomplished by the use of a novel oxidation mask for growing the field oxide isolation. The mask is so designed that its stiffness increases continuously from its outermost edge to its main body over a distance wherein a thick subjacent field oxide narrows towards a silicon active area. The continuously decreasing is flexibility is made possible by a tapered foot at the mask edge. The gradually increasing stiffness towards the main body of the mask permits a smoother transition of stress components than those provided by prior art mask edges which have a foot of uniform thickness. The high flexibility at the mask edge permits the rapidly growing silicon oxide to expand more freely at the mask edge, thereby permitting relief of growth induced stresses. The increasing stiffness towards the main body inhibits the penetration of birds beak.

The oxidation mask is formed by first providing a wafer having a pad

oxide and a thick nitride layer over the pad oxide. A photoresist mask then defines a region wherein a field oxide is to be formed. A thinner nitride layer is formed over the defined region either by thinning the thick nitride layer by partial etching with RIE or by completely etching thick nitride in the region and subsequently depositing a thin nitride layer over the wafer.

A sidewall spacer along the edge of the thick nitride is then formed by the well known technique wherein a layer of material is deposited over the wafer and blanket etched by RIE. The sidewall material used in the preferred embodiments is polysilicon although other materials may also be used. Using the sidewall as a mask, the thin nitride is etched to expose the underlying pad oxide. The tapered nitride foot structure is then formed under the sidewall spacers.

Two methods for forming the tapered foot are presented. In the first method, the tapered foot is formed concurrently with the etching of the thin nitride. In the second method the tapered foot is formed after the thin nitride is etched and during the removal of the sidewall spacer. In the first method a separate process step for the spacer removal is eliminated, thereby improving process efficiency. The second method provides better control of foot length as well as independence of foot length on nitride overetch.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a wafer with a conventional LOCOS oxidation mask before field oxide formation.

Fig. 2 is a cross sectional view of a wafer with a conventional LOCOS oxidation mask after field oxide formation.

Fig. 3 is a cross sectional view of a wafer having a LOCOS oxidation mask with a foot at its edge according to prior art.

Figs. 4 is a cross sectional view of a wafer having a silicon nitride layer over a pad oxide with sidewall spacers in an opening.

Figs. 5A and Fig. 5B are cross sectional views of a wafer showing stages in the formation of a tapered mask foot according a first embodiment of the current invention.

Fig. 6 is a cross sectional view of a wafer after the opening of the thin nitride layer according to the second embodiment of this invention.

Figs. **7A** and Fig. **7B** are cross sectional views of a wafer showing stages wherein the spacer etch simultaneously tapers the mask foot according to a second embodiment of the current invention.

Fig. **8** is a cross sectional view of a wafer after formation of a field oxide region by thermal oxidation using the mask structure of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Fig. **4**, a monocrystalline silicon wafer **40** is provided. A multi-layered oxidation mask is formed by first growing a layer of silicon oxide(pad oxide) **42** to a thickness of about 20 nm. by subjecting the wafer to a clean dry oxidizing ambient in a furnace at about 950°C. A silicon nitride layer **44** between about 50 and 200 nm. thick is then deposited, preferably by low pressure chemical vapor deposition (LPCVD). Using well known photolithographic methods an opening **46** is patterned in the silicon nitride layer **44**. The silicon nitride layer **44** is etched by RIE until the thickness of silicon nitride **44B** within the opening **46** is reduced to between about 30 to 50 nm.

A layer of polysilicon is next deposited to a thickness of between about 50 to 150 nm. and, using a blanket RIE, the sidewall spacers **48** are formed. The methods of forming sidewall spacers are well documented and familiar to those in the art.

The wafer **40** is placed in an RIE tool, for example the LAM 4428x1 manufactured by LAM Research, 4650 Cushing Parkway, Fremont, California 94538, U.S.A. , and etch using well known etchants containing fluorine. Typical etchant chemistries include such gases as SF_6, HBr, CHF_3, and O_2. A

suitable etchant composition in the LAM 4428x1 tool comprises SF_6 at a flow rate of between about 50 and 100 SCCM, CHF_3 at a flow rate of between about 10 and 50 SCCM, and He as a buffer gas used in optimization of the plasma uniformity at a flow rate of between about 100 and 200 SCCM and at an rf power of between 200 and 300 watts. Etch rate ratios of polysilicon-to-silicon nitride of 3:1 or thereabout and appropriate etch profiles can be obtained by optimization of the chamber and plasma conditions using methods well known by those in the art. Similar etch performance can also be achieved by using alternate dry etch methods.

During the etch step, the polysilicon spacer **48** recedes as the thin silicon nitride **44B** within the opening **46** is etched away. Fig. **5A** shows a cross section of the wafer during an intermediate stage of this RIE process step. Because both the silicon nitride and the polysilicon are being etched, the sidewall spacer **48** recedes as the silicon nitride **44B** becomes thinner. This recession is made possible because the sidewall height is never more than about three times the width. Thus curvature of the spacer begins at or very close to its base and the spacer's width begins to recede at or shortly after the onset of etching. As the simultaneous spacer and nitride etching proceeds, a tapered foot **52** forms along the nitride initially covered by the spacer. The dashed line **50** indicates the initial profile.

Fig. 5B shows the wafer cross section after the RIE step has been completed. The spacer **48** has either been completely removed or has receded to insignificant size. The foot **52** forms a nearly smooth transition from its tip to the thick main body **44A** of the nitride layer. The endpoint of the RIE process step is determined when the nitride layer **44B** has been removed within the opening **46**. Excessive over etching must be avoided to prevent the recession of the nitride foot **52**. Any remnants of the spacer **48** need not be removed by an additional etching step. They are converted to silicon oxide during the field oxidation and become a physical part of the oxidation mask. However, they may be removed if desired by a selective etch such as aqueous KOH.

In a second embodiment of this invention a silicon nitride oxidation mask with a tapered foot is formed by first completely etching the silicon nitride within the opening defined by the spacers and then forming a tapered foot by simultaneously etching the spacer and subjacent silicon nitride exposed by the recession of the spacer.

As in the first embodiment, referring again to Fig. **4**, a monocrystalline silicon wafer **40** is provided. A multi-layered oxidation mask is formed by first growing a layer of silicon oxide(pad oxide) **42** to a thickness of about 20 nm. by subjecting the wafer to a clean dry oxidizing ambient in a furnace at about

950°C. A silicon nitride layer **44** between about 50 and 200 nm. thick is then deposited, preferably by low pressure chemical vapor deposition (LPCVD). Using well known photolithographic methods an opening **46** is patterned in the silicon nitride layer **44**. The silicon nitride layer **44** is etched by RIE until the thickness of silicon nitride **44B** within the opening **46** is reduced to between about 30 to 50 nm.

A layer of polysilicon is next deposited to a thickness of between about 50 to 150 nm. and, using a blanket RIE, the sidewall spacers **48** are formed. The methods of forming sidewall spacers are well documented and familiar to those in the art.

The wafer **40** is placed in an RIE tool and etched using a etchant gas comprising SF_6 at a flow rate of between about 50 and 100 SCCM, HBr at a flow rate of between about 10 and 50 SCCM, and O_2 at a flow rate of between about 20 and 50 SCCM, with a carrier gas of helium. The pressure within the chamber is maintained between about 100 and 300 mTorr. During this etch step the polysilicon spacer **48** is durable and does not recede significantly as the thin silicon nitride **44B** is etched away. Over-etching to assure completeness of removal of nitride in the opening is permitted in this embodiment because the foot **52** is protected by the spacer **48**. However, over-etching may nor be

required because additional over-etching of the thin nitride will occur during a second etch step wherein the nitride foot is formed. Fig. **6** shows a cross section of the wafer after the thin nitride layer in the opening **46** has been removed exposing the pad oxide **42**. The nitride foot **52** is defined by the polysilicon spacer **48**.

The spacer **48** is then etched under RIE conditions which etch both nitride and polysilicon, causing the nitride foot **52** to develop a taper as the spacer **48** recedes. A suitable etchant composition in the LAM 4428x1 tool comprises SF_6 at a flow rate of between about 50 and 100 SCCM, CHF_3 at a flow rate of between about 10 and 50 SCCM, and He as a buffer gas used in optimization of the plasma uniformity at a flow rate of between about 100 and 200 SCCM and at an rf power of between 200 and 300 watts. Etch rate ratios of polysilicon-to-silicon nitride of 3:1 or thereabout and appropriate etch profiles can be obtained by optimization of the chamber and plasma conditions using methods well known by those in the art. The duration of the etch is determined by observing endpoint by optical emission spectroscopy. Alternatively a pre-determined etch time interval may be used.

Fig. **7A** shows a cross section of the wafer during an intermediate stage of this RIE process step. Because both silicon nitride and polysilicon are being

etched, the sidewall spacer **48** recedes as the silicon nitride foot **52** develops a taper. This recession is made possible because the sidewall height is never more than about three times the width. Thus curvature of the spacer begins at or very close to its base and the spacer's width begins to recede at or shortly after the onset of etching. The dashed line **50** indicates the initial profile.

Fig. **7B** shows the wafer cross section after the RIE step has been completed. The spacer **48** has either been completely removed or has receded to insignificant size. The foot **52** forms a nearly smooth transition from its tip to the thick main body **44A** of the nitride layer. The endpoint of the RIE step is determined when the tip of the tapered foot **52** has reached a predetermined thickness. Over etching to assure complete removal of nitride in the opening **46** is unnecessary because complete exposure of the opening **46** was assured during the previous RIE step. Any remnants of the spacer **48** need not be removed by an additional etching step. They are converted to silicon oxide during the field oxidation and become a physical part of the oxidation mask. However, they may be removed if desired by a selective etch such as aqueous KOH.

The resultant field oxidation mask formed by the first and second

embodiments are essentially identical as can be seen by comparing Fig. **5B** and **7B**. The choice of method depends upon factors which may relate to circuit design, such as an over etch requirement. An advantage of the second embodiment is that the thickness of the silicon nitride foot at its tip can be better controlled and is essentially independent of any nitride over-etch during the thin nitride etch step.

A field oxide isolation is next grown in a clean oxidation furnace using an ambient gas containing oxygen, either alone or in combination with water vapor, and an optional chlorine containing additive such as trichloroethane to minimized mobile ion contamination. The oxidation temperature is typically between 950°C and 1,100°C. Fig. **8** shows a cross section of the wafer after the field oxide **60** has been formed. The edges of the silicon nitride mask **44A** with the tapered foot **52** have been pushed up by the growth of oxide under the pad oxide.

The growth rate of the field oxide is governed by linear-parabolic kinetics wherein the growth rate is very rapid initially and then slows parabolically according to the diffusion of the oxidizing species. The thin tapered silicon nitride foot **52** flexes and permits the initial rapidly growing silicon oxide expand, thereby providing a means of stress relief which supplements stress relief by

plastic flow. As the oxidation proceeds the growth rate decreases and the stiffer components of the silicon nitride mask come into play, thereby reducing bird beak. Additionally the tapered silicon nitride foot also produces a smooth silicon/silicon oxide profile **62** under the mask edge.

The benefits of an approximately fifty fold reduction in the shear stress component as well as the improved smoothness of edge coverage are realized by this method at the expense of a somewhat longer than conventional birds beak. This birds beak encroachment can be compensated by a lithography bias in the photomask processing. It can also be conveniently removed by a dip etch in dilute HF after the photomask is removed. Narrow channel MOS field effect transistor devices are then fabricated in and over the silicon regions adjacent to the field oxide isolation patterns.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

Whereas in the embodiments cited the thin nitride in the defined region is formed by partially etching the thick nitride through a mask, the thin nitride can

also be formed by etching the thick nitride entirely in the defined region through a mask and then depositing a thin nitride layer over the thick nitride.

CLAIMS

1. A method for forming a field oxide isolation region on a silicon substrate comprising the steps of:

(a) providing a silicon substrate;

(b) forming a pad oxide over said silicon substrate;

(c) forming a silicon nitride layer of a first thickness over said pad oxide;

(d) patterning and partially etching said silicon nitride layer with an anisotropic etching technique, thereby forming a opening and a second thickness of said silicon nitride layer in said opening;

(e) depositing a layer of spacer material on said silicon substrate;

(f) etching said layer of spacer material thereby forming spacers in the periphery of said opening;

(g) simultaneously etching said silicon nitride layer and said spacers with an anisotropic etching technique, whereby a tapered silicon nitride foot is formed under said spacers; and

(h) subjecting said silicon substrate to thermal oxidation, thereby forming said a field oxide isolation region.

2. The method of claim 1 wherein said first thickness of said silicon nitride layer is between about 50 and 200 nm.

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3. The method of claim 1 wherein said second thickness of said silicon nitride layer is between about 30 and 50 nm.

4. The method of claim 1 wherein said layer of spacer material is between about 50 and 150 nm. thick.

5. The method of claim 1 wherein said layer of spacer material is selected from the group consisting of polysilicon and silicon oxide.

6. The method of claim 1 wherein said anisotropic etching technique is reactive ion etching under conditions which provide an etch rate ratio of spacer material to silicon nitride of between about 1:1 and 10:1.

7. The method of claim 1 wherein said local oxide isolation region is between about 300 and 500 nm. thick.

8. A method for forming a field oxide isolation region on a silicon substrate comprising the steps of:

(a) providing a silicon substrate;

(b) forming a pad oxide over said silicon substrate;

(c) forming a silicon nitride layer of a first thickness over said pad

oxide;

(d) patterning and partially etching said silicon nitride layer with an anisotropic etching technique, thereby forming an opening and a a second thickness of said silicon nitride layer;

(e) depositing a layer of spacer material on said silicon substrate;

(f) etching said layer of spacer material thereby forming spacers in the periphery of said opening;

(g) etching said silicon nitride layer thereby exposing said pad oxide within said opening;

(h) simultaneously etching said spacers and said silicon nitride layer exposed thereunder with an anisotropic etching technique, whereby a tapered silicon nitride foot is formed; and

(i) subjecting said silicon substrate to thermal oxidation, thereby forming a field oxide isolation region.

9. The method of claim 8 wherein said first thickness is between about 50 and 200 nm.

10. The method of claim 8 wherein said second thickness is between about 30 and 50 nm.

11. The method of claim 8 wherein said layer of spacer material is between about 50 and 150 nm. thick.

12. The method of claim 8 wherein said layer of spacer material is selected from the group consisting of polysilicon and silicon oxide.

13. The method of claim 8 wherein said anisotropic etching technique is reactive ion etching under conditions which provide an etch rate ratio of spacer material to silicon nitride of 3:1 or thereabout.

14. The method of claim 8 wherein said local oxide isolation region is between about 300 and 500 nm. thick.

15. An oxidation mask for the local oxidation of silicon comprising:

(a) a pad oxide;

(b) a silicon nitride layer over said pad oxide;

(c) an opening in said second silicon nitride layer; and

(f) a silicon nitride foot connected to said silicon nitride layer along the periphery and at the base of said opening, said silicon nitride foot being tapered, and thinning away from said base towards said opening.

16. The oxidation mask of claim 15 wherein said silicon nitride layer is between about 20 and 200 nm. thick.

17. The oxidation mask of claim 15 wherein said opening is between about 350 and 600 nm. wide.