SPECIFICATION

Improvements in television receivers

The present invention relates to improvements in television receivers.

In a known television receiver, in order to form video signals of fixed level which are not affected by the changes of the input signal strength, the gains of a video intermediate frequency amplifier stage and a radio frequency amplifier stage are controlled with an AGC voltage proportional to the peak value of a synchronizing signal. Since an AGC circuit for forming the AGC voltage also responds to noise exceeding the level of a synchronizing signal, a noise canceller is required.

In the case where the noise canceller is designed so that signals exceeding a fixed detection level may be regarded as noise and may have their transmission inhibited or be cancelled, the synchronizing signal is also eliminated by either the arrival of a noise pulse having a large width including the synchronizing signal, or by switching the channel from a broadcasting station of low signal strength to a broadcasting station of high signal strength. As a result, the AGC voltage is reduced, and the corresponding lockout increases the gains of the video intermediate frequency amplifier stage and the radio frequency amplifier stage.

In order to prevent lockout occurring, it has been proposed to employ as means for detecting the noise level, a voltage which is formed by subjecting a composite video signal to a level detection.

However, in this case, since the detection level responds to the width of the noise pulse, there is the disadvantage that the latter part of a noise pulse cannot be eliminated in the case where the width of the noise pulse is great. When the time constant for the level detection is made sufficiently great, the same lockout as in the noise cancelling based on the fixed level above described temporarily occurs. Therefore, the time constant cannot be made very great.

In noise detection based on the level detection voltage, accordingly, although the lockout can be prevented, the operation of a synchronizing circuit is disturbed by the inoperative state of the noise canceller as described above and the AGC voltage is adversely affected by the noise.

Furthermore, in the case where the noise canceller is to be contained in a monolithic semiconductor integrated circuit, it increases the number of external terminals required and also the number of external components in order to constitute the time constant circuit required for the level detection. On the other hand, when the time constant circuit is contained in the monolithic semiconductor integrated circuit, the problem arises that the density of integration is substantially reduced on account of the space occupied by a capacitor of large capacitance.

It is an object of the present invention to provide a television receiver equipped with a noise canceller which performs a reliable noise cancelling operation whilst preventing lockout from occurring.

According to the present invention there is provided a television receiver including

(a) a video intermediate frequency amplifier which amplifies a video intermediate frequency signal;

(b) a video detector which receives an output signal of said video intermediate frequency amplifier at its input and thereby provides a composite video signal from its output;

(c) a noise canceller which cancels noise in said composite video signal;

(d) an AGC detector which receives an output signal of said noise canceller at its input and thereby provides from its output an AGC voltage for controlling the gain of said video intermediate frequency amplifier;

(e) a vertical oscillator which is substantially controlled by a vertical synchronizing pulse in said composite video signal; and

(f) means controlled by a pulse provided from said vertical oscillator, thereby to control a noise cancelling operation of said noise canceller associated with the operation of said AGC detector into an inoperative state during the vertical flyback time.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:

Figure 1 is a block diagram of a preferred form of television receiver; and

Figure 2 is a circuit diagram showing the details of the relevant components of the television receiver shown in Figure 1.

Referring first to Figure 1, the television receiver is shown as a simplified block diagram. It should be noted that the circuit components enclosed with a dotted line are formed within a single semiconductor silicon chip by the well-known method of producing a monolithic semiconductor integrated circuit device, and that the reference numerals enclosed with circles indicate terminal numbers.

The television receiver includes first, second and third video intermediate frequency amplifiers 1, 2 and 3 respectively, which amplify a video intermediate frequency input signal IF_{IN} applied across terminals 25 and 26. Capacitors C_{36} and C_{37} respectively connected to terminals 23 and 24 are arranged between the two lines of a D.C. feedback circuit and earth, the feedback circuit being between the video intermediate frequency amplifiers 3 and 1.

An output signal from the video intermediate frequency amplifier stage comprising the amplifiers 1 to 3 is applied to a video detector 4 through a high-pass filter consisting of capacitors C_1 and C_2 and resistors R_1 and R_2. The high-pass filter is provided in order to prevent an audio intermediate frequency signal of 4.5 MHz being developed in the video intermediate frequency amplifier due to crosstalk through a power supply line from an audio circuit to be described later.

A coil L_{10} and a capacitor C_{10} each connected

across terminals 27 and 28 constitute a tank circuit which is tuned to 58.75 MHz.

A video detection output signal from the detector 4 is amplified by a video amplifier 5, and is delivered from a terminal 3 through an output buffer amplifier 6 which also serves for as an additional noise cancelling device. The terminal 3 is connected through a filter F_1 which acts as a sound trap for various circuits at the succeeding stage, for example, a video amplifier stage or a band-pass amplifier in a colour television receiver. The filter F_1 comprises resistors R_{10} and R_{11} and ceramic capacitances as shown.

The output signal of the video amplifier 5 is applied to a noise canceller 7 and an AGC detector 8.

The noise canceller 7 executes a noise cancelling operation in such a way that noise is detected on the basis of a fixed noise detection level and that an inverted noise signal is transmitted to the output buffer circuit 6, in order to cancel any noise in the output video signal. With regard to the AGC detector 8, the noise detection output is added to a synchronous pulse detection output which is inverted by the AGC detector, in order to cancel noise included in the synchronous pulse detection output.

A capacitor C_{34} and a resistor R_{41} connected to terminal 21 constitute a time constant circuit for the AGC detection.

An AGC voltage formed by the AGC detector 8 is used for the gain controls of the video intermediate frequency amplifiers 1 to 3. The AGC voltage is also applied to an AGC amplifier 9 for forming an AGC voltage of a radio frequency amplifier stage. The AGC voltage to the radio frequency amplifier stage is delivered from terminal 22. A variable resistor R_{40} connected to a terminal 20 is provided in order to adjust the starting level of the AGC operation of the radio frequency amplifier stage.

The composite video signal obtained from the terminal 3 is applied through a circuit comprising a series resistor R_{15}, and parallel arranged resistor R_{16} and capacitor C_{19} and through a terminal 9 to a synchronous separator 10, in which horizontal and vertical synchronous pulses are extracted.

The resulting synchronous separation output is applied to an AFC circuit 11. The AFC circuit 11 detects the phase difference between the output pulse of the synchronous separator 10 and a flyback pulse FBP applied to a terminal 11 through a resistor R_{17} and a capacitor C_{22}. The phase difference signal is smoothed by an integrating circuit connected to a terminal 12, to form an AFC voltage.

The AFC voltage is applied to a horizontal oscillator 12 through terminal 12 so as to bring the oscillation frequency of the horizontal oscillator 12 and the frequency of a horizontal synchronous signal into agreement. The resulting oscillation output is delivered from a terminal 19 through a horizontal driving amplifier 13.

By applying the synchronous separation output signal delivered from a terminal 10 to an integrating circuit, the vertical pulse is extracted and is applied through a terminal 14 to a vertical synchronous trigger circuit 14, which controls the oscillation frequency of a vertical oscillator 15.

An output signal from the vertical oscillator 15 is applied to a vertical driving amplifier 16, the output of which is delivered through a terminal 18 so as to drive a push-pull output circuit having transistors Q_1 and Q_2, resistors R_{28} to R_{39}, capacitors C_{31} to C_{33}, a diode D_{10} and a coil D_y.

A part of an output signal from this vertical output circuit is fed back to the vertical oscillator 15 and the vertical driver 16 through terminals 16 and 17 respectively. A time constant circuit which constitutes the vertical oscillator is connected to a terminal 15.

The noise cancelling operation of the noise canceller 7 is rendered ineffective by the oscillation pulse of the vertical oscillator 15 during a vertical flyback time.

The audio intermediate frequency signal from the terminal 3 is applied to terminals 4 and 5 through a filter F_2 which passes the audio intermediate frequency signal of 4.5 MHz. The filter F_2 includes a coil L_{12} a capacitor C_{13} and ceramic capacitors as shown. The output of a limiter amplifier 17 is applied to an FM detector 18 through a coupling capacitor C_3. A phase shifter in the form of a tank circuit, which constitutes part of the FM detector is connected to terminals 6 and 7. This phase shifter includes coils L_{13} and L_{14}, and capacitors C_{15} to C_{17}.

An FM detection output from the FM detector 18 is amplified by an audio amplifier 19 and is delivered from a terminal 8.

Figure 2 is a detailed circuit diagram showing the essential parts of the basic circuit illustrated in block form in Figure 1.

The video amplifier 5 has its inputs supplied with detection signals which are outputs on output lines 41 and 42 of the video detector 4 and which are opposite in phase to each other.

The detection output signals are applied to the base electrodes of transistors Q_{50} and Q_{52} whose emitter electrodes are connected to transistors Q_{58} and Q_{59} respectively, which transistors constitute constant current source circuits. The output from the emitter electrode of the transistor Q_{50} is applied to the base electrode of a p-n-p transistor Q_{51}, whilst the output from the emitter electrode of the transistor Q_{52} is applied to the base electrode of a p-n-p transistor Q_{53}. The output from the collector electrode of the transistor Q_{53} is applied to the collector electrode of the transistor Q_{51} through a current mirror circuit which is constituted by transistors Q_{54} and Q_{55} and resistors R_{56} and R_{57}.

The composite video amplified signal as added is amplified by a common-emitter type amplifier which is constituted by a transistor Q_{56}. The amplified output is applied firstly to the base electrode of a transistor Q_{60} constituting an emitter follower circuit, and secondly to the output buffer circuit 6 through a resistor R_{61}.

The output buffer circuit comprises an emitter

follower transistor Q_{62}, a transistor Q_{63} which constitutes a constant current source and which is connected to the emitter electrode of the transistor Q_{62}, a transistor Q_{64} whose collector and emitter electrodes are respectively connected in common with the corresponding electrodes of the transistor Q_{62}, and a resistor R_{69} and a forward diode Q_{65} which are connected in series between the base and collector electrodes of the transistor Q_{64}. A noise cancelling transistor Q_{66} is located between earth and the common junction of the resistor R_{69} and the diode Q_{65}.

The noise canceller 7 comprises differential transistors Q_{67} and Q_{68} for noise detection, a transistor Q_{69} which constitutes a constant current source circuit and which is connected to the common emitter electrodes of the transistors Q_{67} and Q_{68}, and output transistors Q_{70} and Q_{71}.

The base electrode of one differential transistor Q_{67} is supplied through a resistor R_{73} from the emitter follower transistor Q_{60} of the video amplifier 5 with the composite video signal whose audio intermediate frequency component has been removed by a high-pass filter constituted by the resistor R_{73} and a capacitor C_{50}. The base electrode of the other differential transistor Q_{68} is supplied with a noise detecting reference voltage which is a constant voltage to be described later.

The inverted noise detection output signal provided from the transistor Q_{67} of the noise canceller 7 is applied to the base electrode of the transistor Q_{70}, the collector electrode of which has a diode Q_{72} connected thereto. This diode Q_{72} constitutes a current mirror circuit along with the transistor Q_{68}. The non-inverted noise detection output signal provided from the transistor Q_{68} is applied to the base electrode of the transistor Q_{71}. A diode Q_{73} and a transistor Q_{65} which are connected to the collector electrode of the transistor Q_{71} constitute a current mirror circuit, and are used for the cancellation of noise within the AGC detector 8.

A stabilized voltage provided by a Zener diode ZD and a resistor R_{77} is divided by a resistor R_{78}, a diode Q_{78} and a resistor R_{79}. The junction between the resistor R_{78} and the diode Q_{78} is connected to the base electrode of a constant current transistor Q_{77}. A constant current provided by this transistor Q_{77} is caused to flow through resistors R_{80} and R_{81}, whereby constant voltage drops are formed.

The voltage drop across the resistor R_{81} is applied to the base electrode of a transistor Q_{75}, the emitter electrode of which provides the noise detecting reference constant voltage for the noise canceller 7.

The AGC detector 8 comprises differential transistors Q_{79} and Q_{80} and a constant current transistor Q_{81} similar to those of the noise detector, and an output transistor Q_{82}.

However, a detecting reference voltage for detecting the synchronous signal is set to be higher than the noise detecting reference voltage by the voltage drop across the resistor R_{81}. On the input side of the AGC detector 8, there are arranged a resistor R_{91} and a capacitor C_{51} which constitute a high-pass filter. The inverted synchronous signal provided from the collector electrode of the transistor Q_{79} is applied to the output transistor Q_{82}. A current mirror circuit constituted by a diode Q_{83} and transistor Q_{84} is connected to the collector electrode of the output transistor Q_{82}, whereby the synchronous signal is provided from the collector electrode of the transistor Q_{84}. The output from the collector electrode of the transistor Q_{84} is subjected to a level detection by the base and emitter electrodes of a transistor Q_{86}, a resistor R_{94}, and a time constant circuit consisting of the resistor R_{41} and the capacitor C_{34}, connected to the terminal 21, so that the AGC voltage is formed.

A noise cancelling transistor Q_{85} is arranged in parallel with the transistor Q_{84} for obtaining the inverted synchronizing signal.

A transistor Q_{87} which is controlled by the output pulse of the vertical oscillator 15 and which turns "on" in the vertical flyback time is incorporated between the base and emitter electrodes of the noise cancelling transistor Q_{85}.

The operation of the circuits described above will now be described in greater detail. On account of the composite video signal V_{comp} of negative polarity from the video amplifier 5, the AGC detector 8 also responds to a negative voltage signal V_N exceeding the noise detection voltage V_S. At this time, however, the transistor Q_{85} turns "on", so that an inverted noise pulse going to become a high level is nullified.

In the case where the fixed noise detection reference voltage disclosed in the prior art is used, the lockout as described above arises. However, in the embodiment described above, the transistor Q_{87} turns "on" during the vertical flyback time and functions to turn "off" the noise cancelling transistor Q_{85}. Accordingly, even when the lockout has occurred temporarily due to, e.g. channel switching, the interruption of the noise cancelling operation in the vertical flyback time permits the formation of the AGC voltage proportional to the peak value level of the synchronous signal during the time. Therefore, the AGC voltage rises gradually, and the lockout can be automatically released.

The features to be especially noted in the above described embodiment are as follows:

(a) The noise canceller 7 is completely contained in the monolithic semiconductor integrated circuit, and the time constant circuit for detecting the signal level previously used is not arranged in this noise canceller 7.

(b) Since the time constant circuit for detecting the signal level is omitted from the noise canceller 7, the noise cancelling operation of the noise canceller 7 is executed with reference to the fixed detection level.

(c) Since the oscillation pulse of the vertical oscillator 15 is applied to the noise canceller 7, the noise cancelling operation of the noise canceller 7 is interrupted during the vertical flyback time.

Thus the above features not only prevent the

lock-out occurring, but also reduce the external terminals and external components of the monolithic semiconductor integrated circuit.

On the basis of the above, the lockout can be prevented by the intermittent inoperative states of the noise canceller in only the vertical flyback time and the noise cancelling operation based on the fixed detection level can be performed, so the noise cancelling is reliable.

Owing to the reliable noise cancelling operation, synchonism disturbances etc. are not caused by wide pulses, and any substantial synchronism disturbance influential on a picture is not caused by noise in the vertical flyback time, either. In the presence of noise in the vertical flyback time, the AGC voltage responds thereto, but the influence of the noise does not remain in the video signals which form an effective picture on the basis of the AGC voltage after the end of the vertical flyback time and free from noise.

Furthermore, in the case where the noise canceller and the vertical oscillator are formed within the identical monolithic semiconductor integrated circuit as illustrated in Figure 1, the time constant circuit for forming the noise detection level as stated before can be dispensed with and both can be directly coupled within the integrated circuit, so that the number of the external terminals and the external components can be reduced or that the lowering of the density of integration can be prevented.

In a modified form, the noise cancelling operation may well utilize an analog switch circuit which inhibits the transmission of the composite video signal.

Various circuit blocks which constitute the television receiver are usually constructed of monolithic semiconductor integrated circuits, and their combination can be modified as appropriate. For example, the audio circuit 19 could be formed in another monolithic semiconductor integrated circuit.

However, it is desirable that the noise canceller and the vertical oscillator are formed in the identical monolithic semiconductor integrated circuit as described above, in order to achieve a reduction in the number of external terminals.

CLAIMS

1. A television receiver including:

(a) a video intermediate frequency amplifier which amplifies a video intermediate frequency signal;

(b) a video detector which receives an output signal of said video intermediate frequency amplifier at its input and thereby provides a composite video signal from its output;

(c) a noise canceller which cancels noise in said composite video signal;

(d) an AGC detector which receives an output signal of said noise canceller at its input and thereby provides from its output an AGC voltage for controlling the gain of said video intermediate frequency amplifier;

(e) a vertical oscillator which is substantially controlled by a vertical synchronizing pulse in said composite video signal; and

(f) means controlled by a pulse provided from said vertical oscillator, thereby to control a noise cancelling operation of said noise canceller associated with the operation of said AGC detector into an inoperative state during the vertical flyback time.

2. A television receiver according to claim 1, wherein said noise canceller and a part of said vertical oscillator are formed within a single monolithic semiconductor integrated circuit.

3. A television receiver constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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(e) a vertical oscillator which is substantially controlled by a vertical synchronizing pulse in said composite video signal; and

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