# MICROPROCESSOR WITH IMPROVED OUT OF ORDER SUPPORT VIA REGISTER MANAGEMENT WITH SYNCHRONIZATION OF MULTIPLE PIPELINES

ABSTRACT

A system and method for synchronization of multiple pipelines providing for processing a stream of instructions in a computer having a first (200, 200', 200") and a second (202, 202', 202") processing element, each element having its own state determined by a setting of its own registers. When processing said stream by said first processing element (200, 200', 200") it becomes beneficial to have said second processing element (202, 202', 202") begin processing of the same instruction stream, then the first (200, 200', 200") and second (202, 202', 202") processing elements process the stream of instructions, but only one of said processing elements is permitted to change the overall state of said computer system. The second processor (202, 202', 202") has more pipeline stages than the first (200, 200', 200") in order to feed the first processor (200, 200', 200") and reduce the finite cache penalty and increase performance. In an alternative embodiment the foregoing process is generalized allowing processors to forward and store state changes for future use as required by the other processor.

Fig. 2