FIG. 1

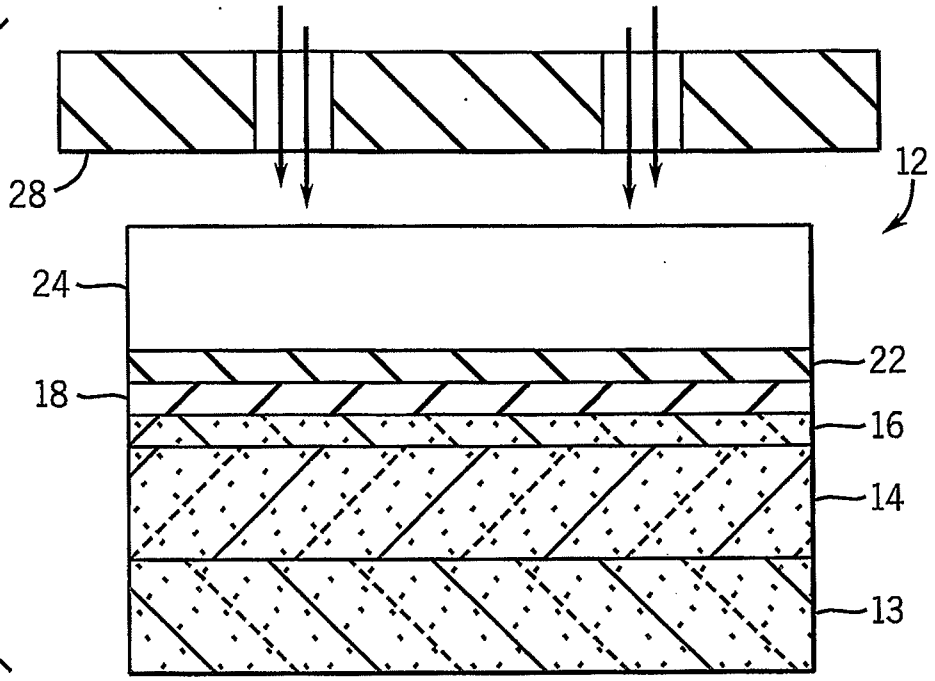


FIG. 2

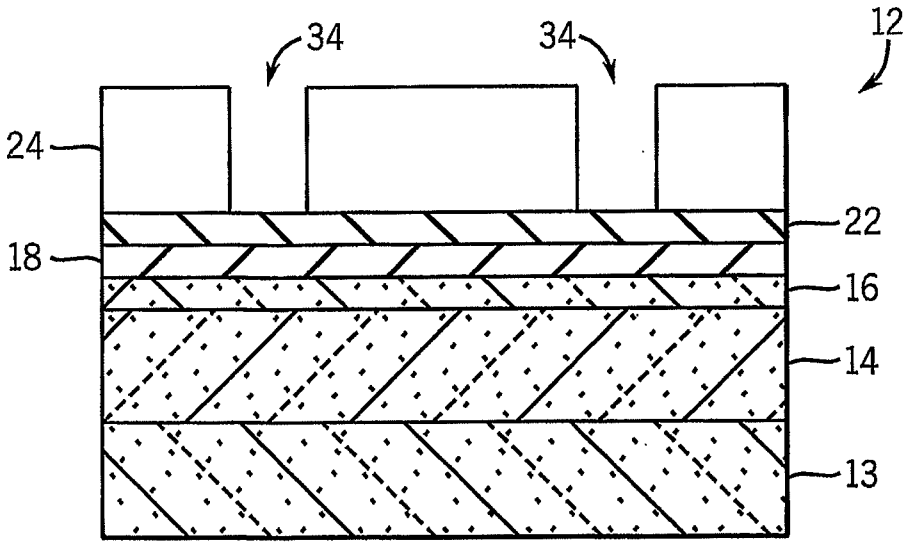


FIG. 3

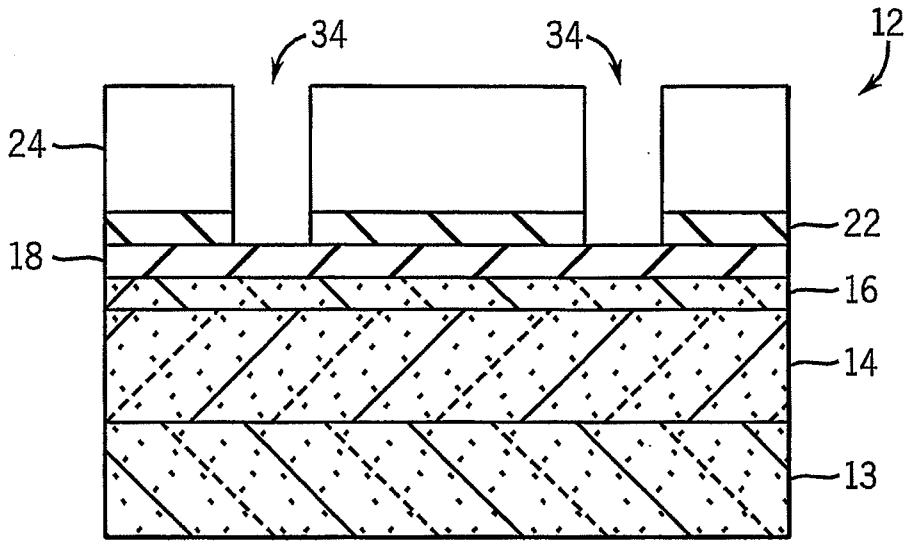


FIG. 4

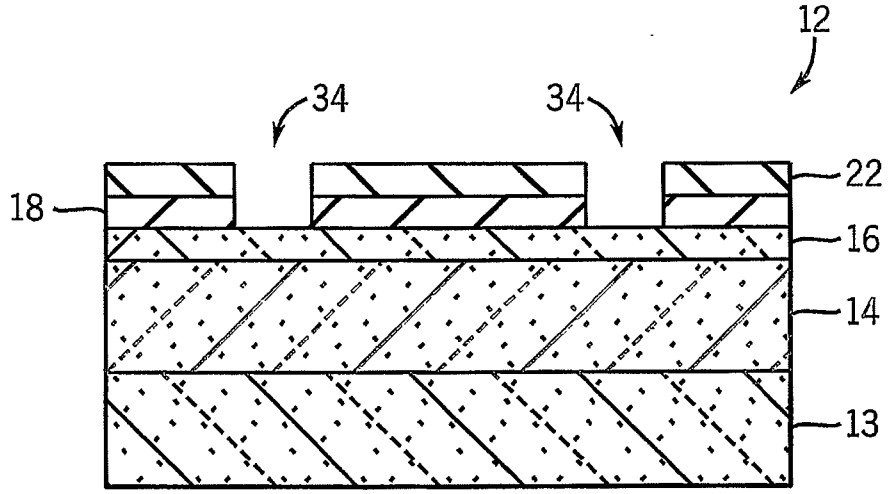


FIG. 5

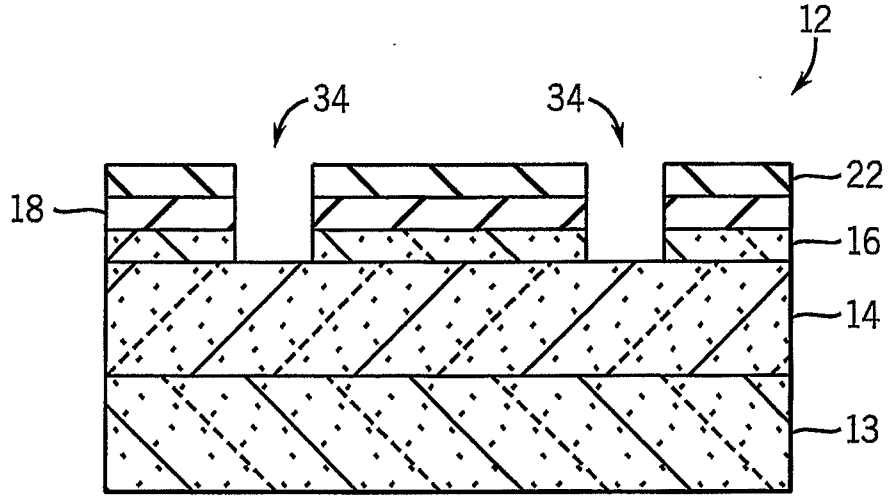


FIG. 6

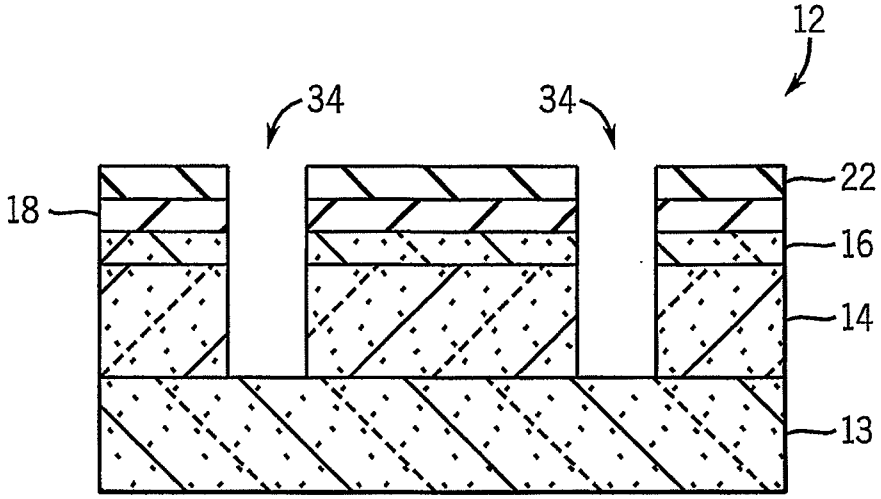


FIG. 7

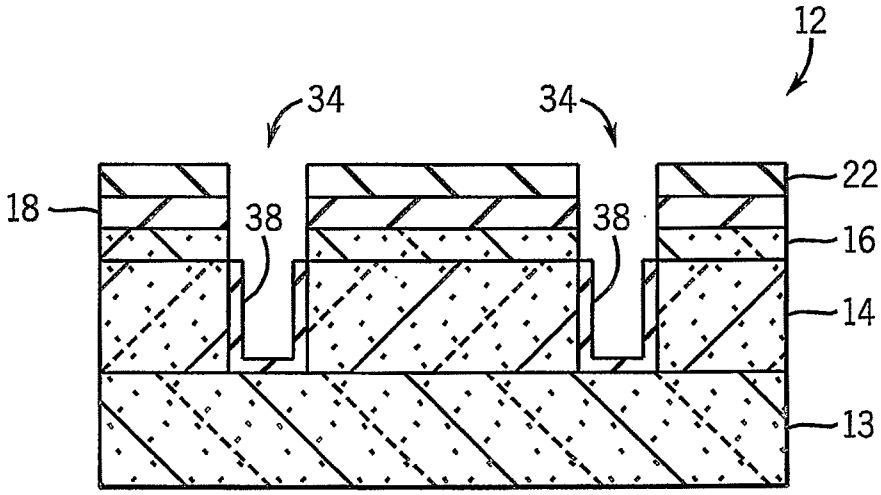
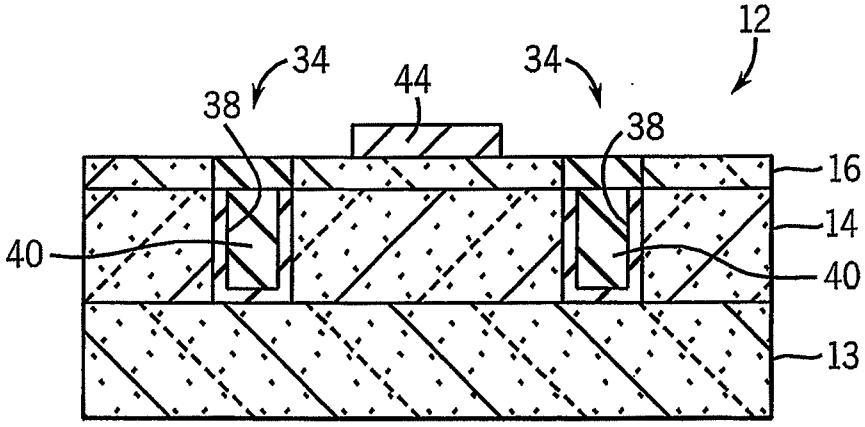


FIG. 8



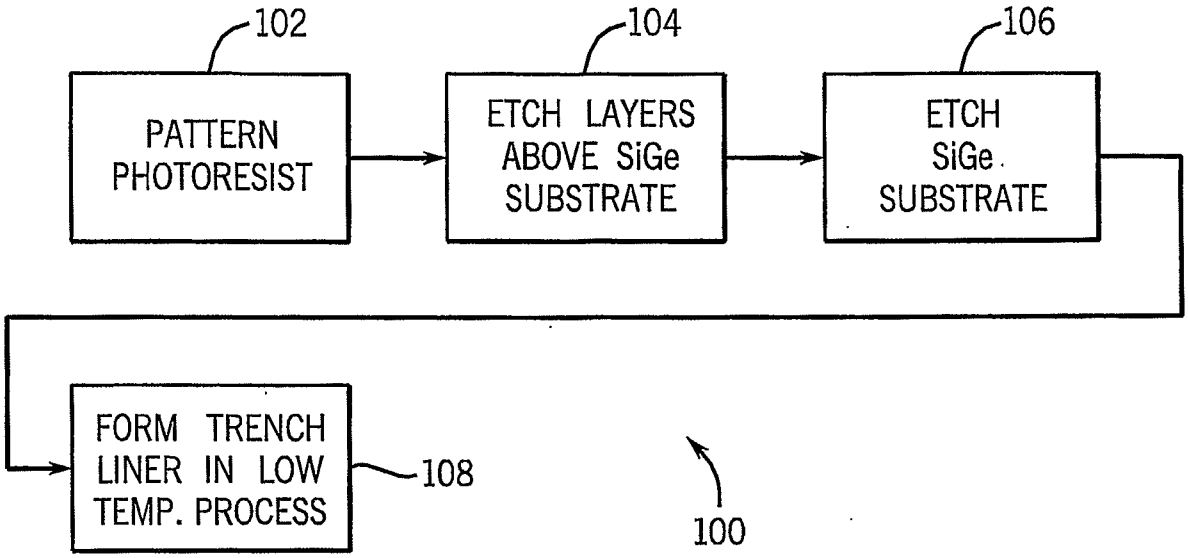

102
PATTERN PHOTORESIST
104
ETCH LAYERS ABOVE SiGe SUBSTRATE
106
ETCH SiGe SUBSTRATE
FORM TRENCH LINER IN LOW TEMP. PROCESS
108
100

FIG. 9

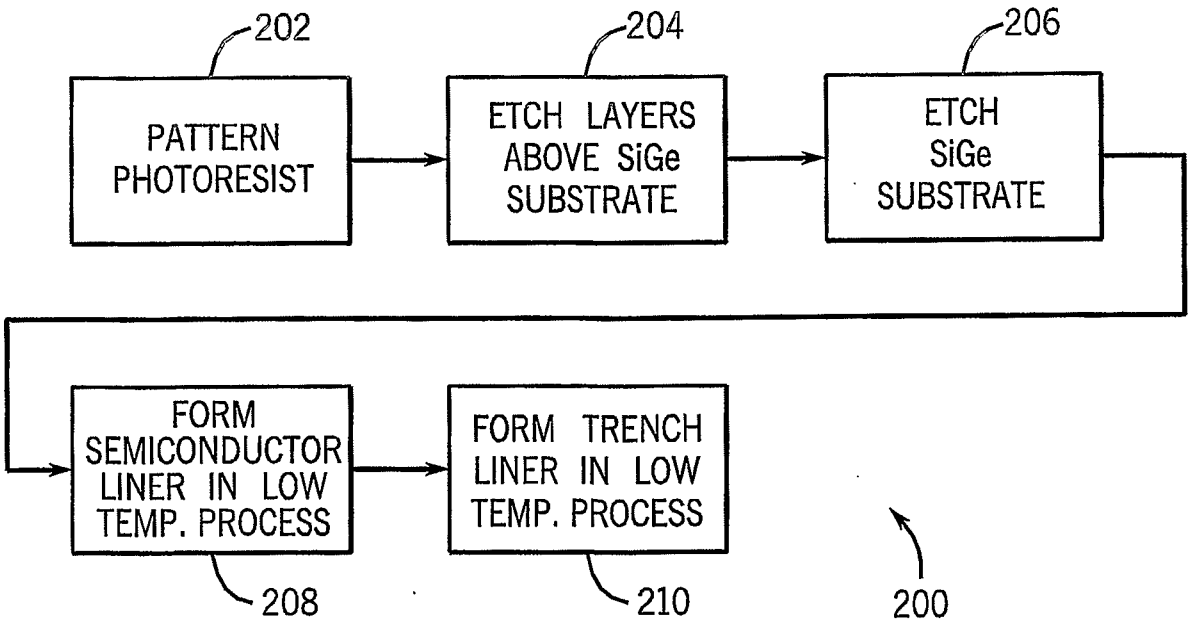

202
PATTERN PHOTORESIST
204
ETCH LAYERS ABOVE SiGe SUBSTRATE
206
ETCH SiGe SUBSTRATE
FORM SEMICONDUCTOR LINER IN LOW TEMP. PROCESS
208
FORM TRENCH LINER IN LOW TEMP. PROCESS
210
200

FIG. 21

FIG. 10

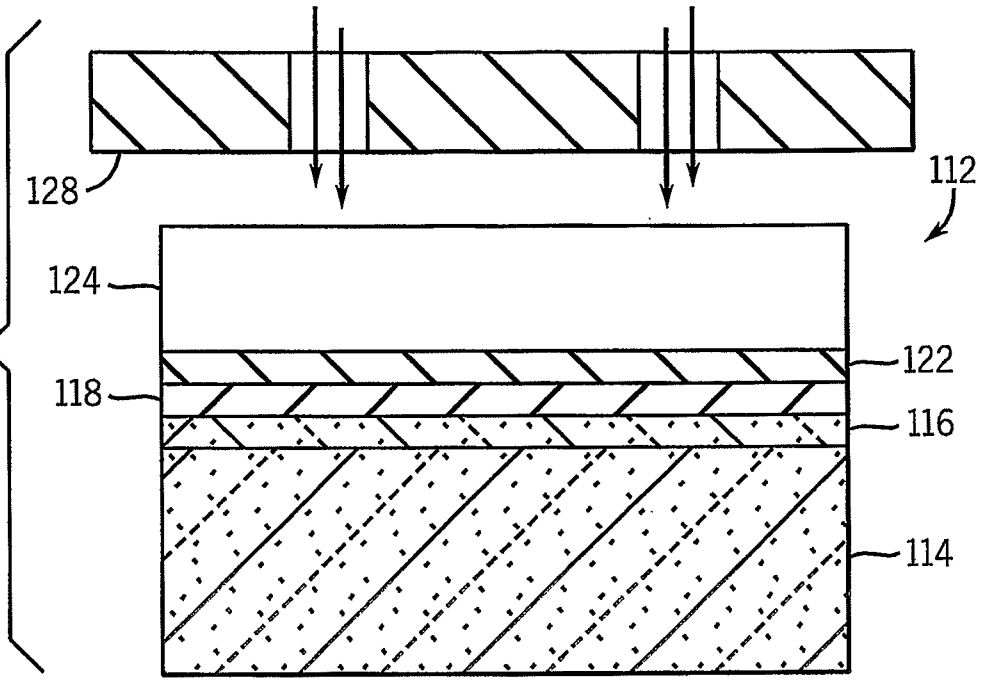


FIG. 11

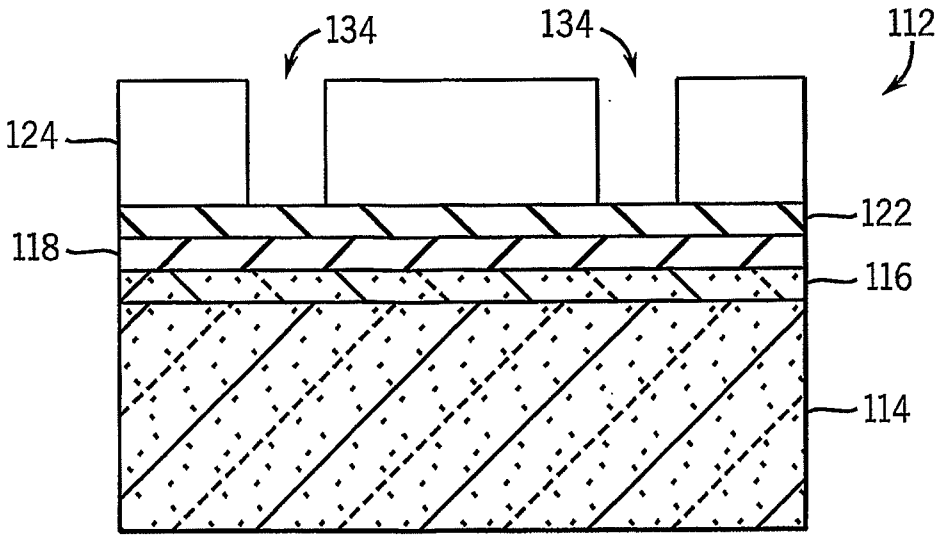


FIG. 12

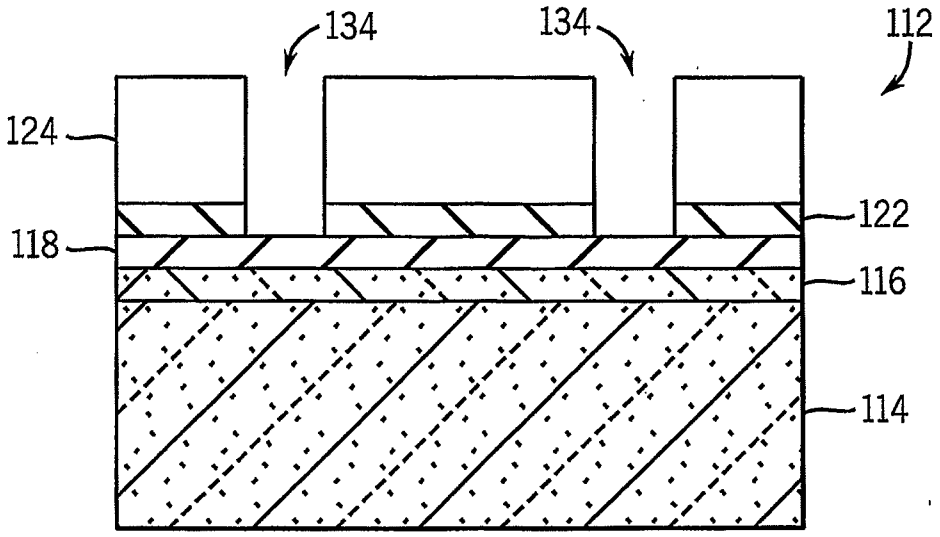


FIG. 13

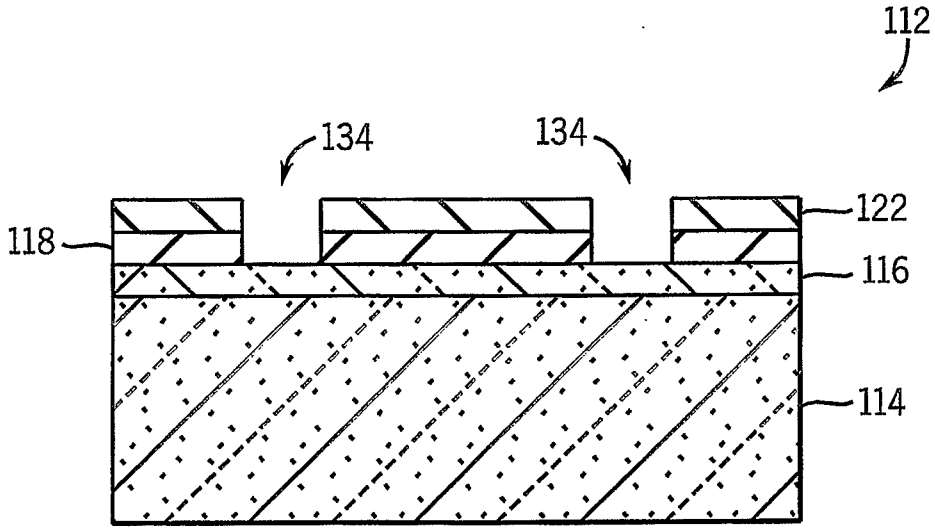


FIG. 14

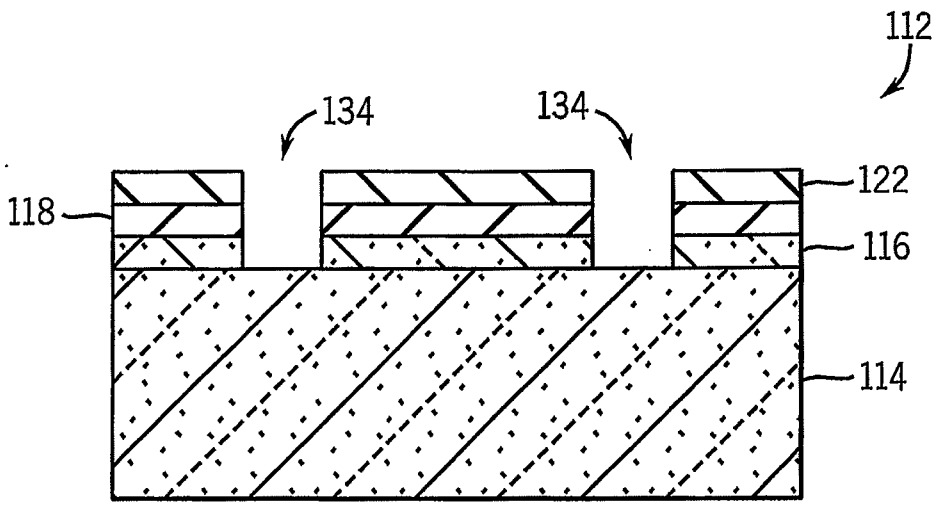


FIG. 15

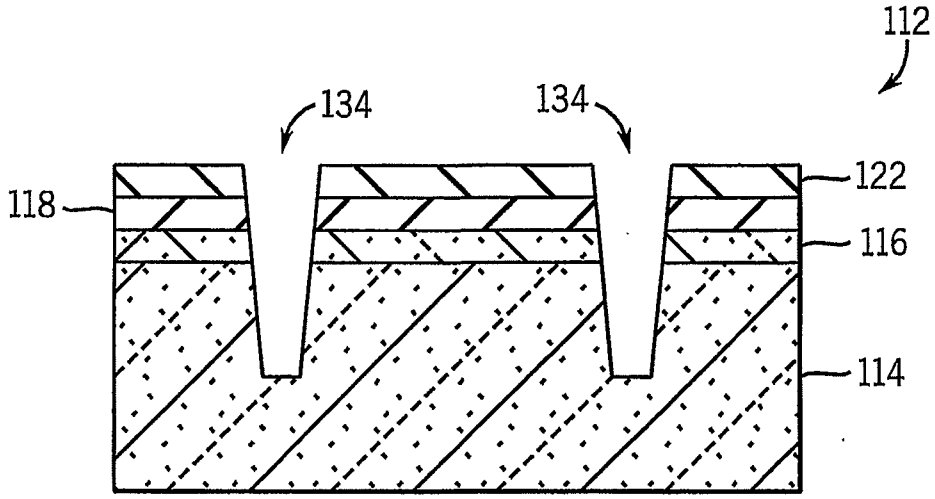


FIG. 16

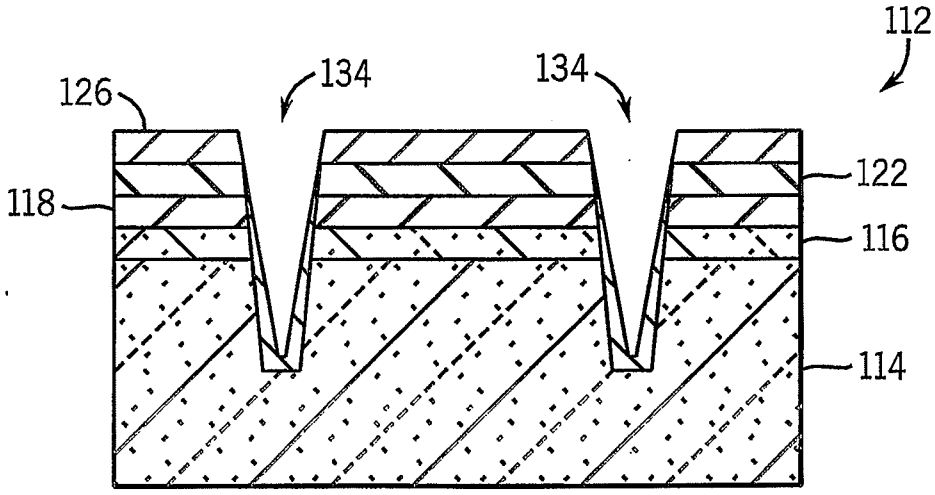


FIG. 17

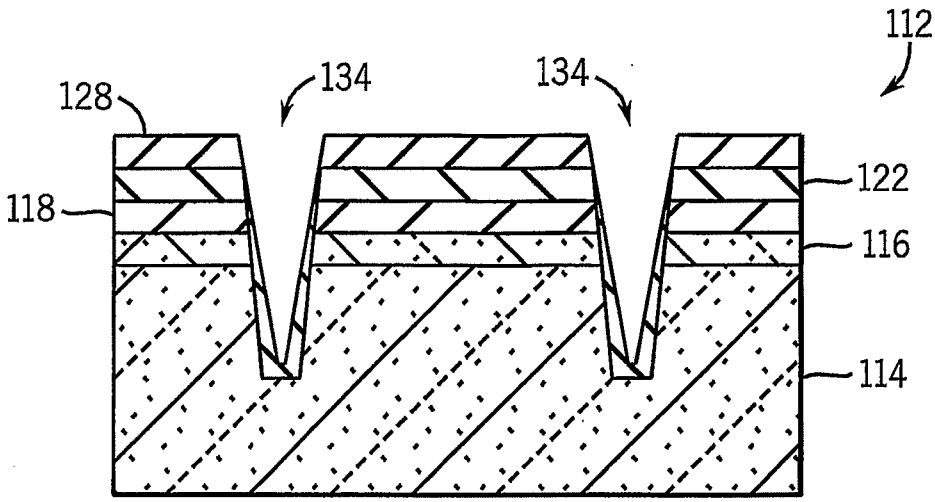


FIG. 18

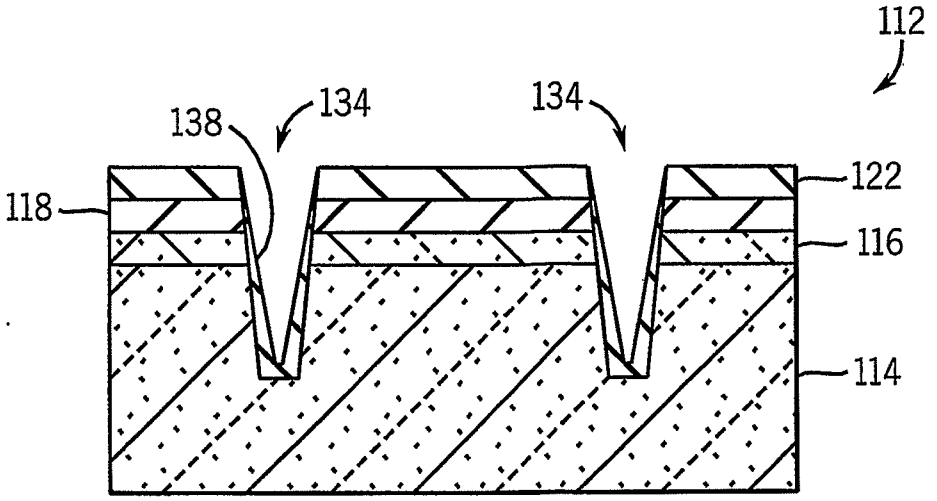


FIG. 19

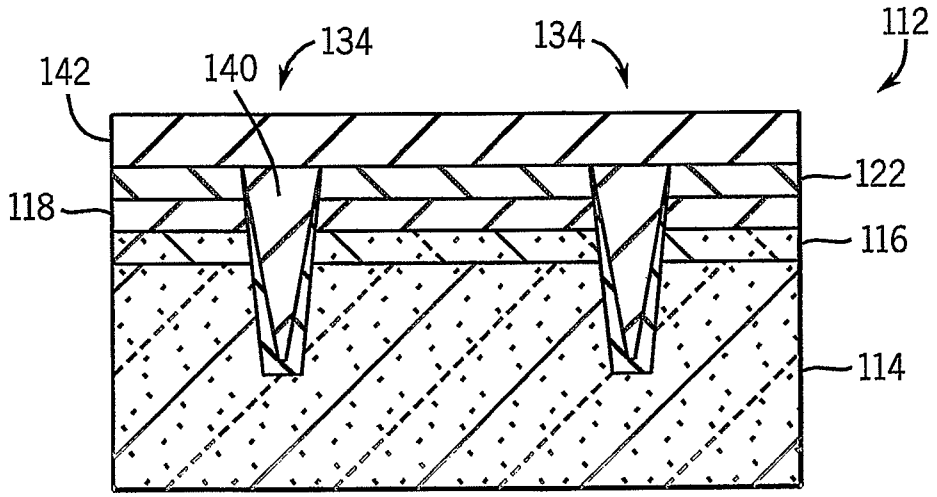


FIG. 20

