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(54) SEMICONDUCTOR DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices comprising a semiconductor body on a surface of which extends a conductive track which is secured to and insulated from the semiconductor body over at least part of its length by means of an insulating material, said conductive track comprising first and second metal layers of different materials which are connected locally via an interposed third metal layer, the material of the third metal layer differing from that of the first and that of the second metal layers and forming therewith with stable low-ohmic junctions.

As is known, conductive tracks are frequently used in semiconductor devices for interconnection and/or contacting purposes; such tracks extend over a protective insulating layer; at apertures in the insulating layer the conductive tracks can be connected to regions of semiconductor circuit elements of the semiconductor body. The materials of which the conductive tracks consist must exhibit particular properties. Contacts between the conductive track and the semiconductor body usually must be non-rectifying and must show a low series resistance. The insulating layer must readily adhere to the semiconductor body surface, and a good adherence between the conductive track and the insulating layer also is an important requirement. The material of at least the major part of the conductive track must have a high conductivity, and, for example, the etchability and the suitability for adhering connection conductors are of great importance, as well as the temperature stability both in connection with the operations to be performed in the manufacture of the device after providing the conductive track and the operating temperatures of the device.

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In practice the multiplicity of requirements imposed on the conductive track material, a number of which have been mentioned by way of example, has resulted in the use of conductive tracks of which various parts are manufactured from different materials. In one known construction, the part of the conductive track which contacts the semiconductor body consists of aluminium, and the contact surfaces for connection conductors, which often consist of gold, are of gold. In such a case, an additional important requirement is that the junction between the various metals of the conductive track is stable and low-ohmic.

When various metals of such a composite conductive track contact each other directly, the stability of the resulting junction is, in many cases, undesirably low. A known example is the junction between aluminium and gold, in which intermetallic compounds are easily formed at the junction and have a serious adverse influence on the quality of the junction.

In "E.E.E. The Magazine of Circuit Design Engineering" Volume 16, No. 5, page 36, it is proposed to increase stability by means of an intermediate layer. In this case the conductive track consists mainly of aluminium which is particularly suitable for the purpose and is furthermore covered with an insulating layer. At the region of the contact surfaces, apertures are provided in the insulating layer, so that at this region the aluminium is exposed. In these apertures a layer of titanium and then a layer of gold are provided. On these resulting gold contact surfaces gold connection conductors can easily be provided, the gold and the aluminium being separated from each other by the interposition of the titanium, so that the formation of gold aluminium compounds is counteracted.

However, in a semiconductor device having such a known composite conductive track, in

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which the two metals of the track are connected via an interposed third metal, the quality of the connection between the first and the second metal is not sufficient for all applications, since direct contact between the materials of the first and second metal layers can still occur by diffusion at pin-holes in the interposed third metal layer and at the edges of the apertures in which the third metal layer is provided.

According to the invention a semiconductor device comprises a semiconductor body on a surface of which extends a conductive track which is secured to and insulated from the semiconductor body over at least part of its length by means of an insulating material, said conductive track comprising first and second metal layers of different material which are connected locally via an interposed third metal layer, the material of the third metal layer differing from that of the first and that of the second metal layers and forming therewith stable low-ohmic junctions, the projections on the semiconductor body surface of the junctions between the first and third metal layers and the second and third metal layers being juxtaposed.

In this manner, direct contact between the first and second metal layers through pin holes in the interposed third metal layer can be prevented. It has been found that particularly stable and low-ohmic junctions can be obtained by such a lateral separation.

Especially, for example, in semiconductor devices in which one or more semiconductor regions of a semiconductor circuit element of the semiconductor body are to be connected to parts of an envelope via connection conductors, the use of composite conductive tracks is often very desirable, for example the said parts of the envelope are often of gold or at least are often gold-plated; although gold is less suitable for the parts of the conductive track forming ohmic and stable contact with the semiconductor regions. It will be obvious that it is desirable in this case to employ that in a composite track which has a stable junction and can be obtained in a simple manner. Thus, in a semiconductor device in accordance with the invention, the semiconductor body may comprise two or more regions of opposite conductivity type associated with a semiconductor circuit element, at least one of the said regions being connected to the first metal layer at an aperture in the insulating material, the second metal layer being provided with a connection conductor.

The surface area of the junction between the second and the third metal layer may be small compared with the overall surface area of the second metal layer.

The invention can be used advantageously in semiconductor devices having a multi-level conductive track which includes several layers

one above the other, for example, in integrated circuits which have a large number of circuit elements.

A plurality of layers of insulating material may be present at the surface of the semiconductor body, the second metal layer extending substantially entirely on the free surface of the uppermost insulating layer and being connected via at least one aperture in the uppermost insulating layer and via the third metal layer to the first metal layer which is situated substantially entirely between two of the said insulating layers.

The material of the part of the conductive track which is situated on the uppermost layer can be chosen with a view to the necessary connections to parts of an envelope or to parts of other semiconductor devices, which is of particular importance because the number of connections in semiconductor devices of this type can be very large so that extra high requirements must be imposed upon the reliability of these connections. The metal of the second metal layer can be adapted to the methods to be used for making such connections; such methods include, for example, the use of parts the thickness of which has been increased, usually by electro-deposition, and which project above the free surface insulating layer, i.e. in a direction perpendicular to the semiconductor surface. The conductive track may comprise at least one part which is associated with the second metal layer, is thicker than the first metal layer and projects laterally, i.e. substantially parallel to the semiconductor surface, beyond the semiconductor body. Such thickened parts may be so called "beam-lead" structures.

By such thickened parts it becomes possible, for example, to produce the hereinbefore necessary connections simultaneously in one operation; this can be of importance from the point of view of manufacture.

The junction between the first and third metal layers and that between the second and third metal layers may be situated at least for the greater part on the same side of the third metal layer. Particularly stable junctions can be obtained in a simple manner when the two junctions are situated at least for the greater part on the side of the third metal layer remote from the semiconductor body, the third metal layer extending entirely on an insulating layer situated between the semiconductor surface and the uppermost insulating layer.

The material of the various metal layers may be both substantially pure metals and alloys. Aluminium may be chosen as particularly suitable for the first metal layer, and copper and in particularly gold for the second metal layer.

The material for the third metal layer which is preferably substantially impermeable to the materials of the first and the second

metal layer, may be, for example, molybdenum, platinum, nickel, tungsten, or rhodium.

5 It is to be noted that the properties of a contact between a semiconductor region and the first metal layer can be improved, if desired, by using a suitably chosen surface concentration in the semiconductor region to be connected, which concentration can also
10 be obtained, for example, by means of an extra diffusion treatment. The said contact can also be improved by using special materials, such as cobalt- and platinum silicide in the contact window.

15 The adherence between one or more of the metal layers and the adjoining insulating material can be improved, if desired, by using thin adhering layers. These adhering layers may consist of, for example, aluminium, or platinum silicide, or such materials as
20 titanium, chromium, molybdenum, niobium, cobalt and nickel.

Embodiments of the invention will now be described by way of example, with reference
25 to the accompanying diagrammatic drawing in which:—

Figure 1 is a cross-sectional view of a semiconductor device in accordance with the invention;

30 Figure 2 is a cross-sectional view of a part of a second semiconductor device in accordance with the invention, and

35 Figure 3 is a cross-sectional view of a part of a third semiconductor device in accordance with the invention.

The semiconductor device shown in Figure 1 is a discrete bipolar transistor. This transistor comprises a semiconductor body 1 which is formed by a substrate 2 on which
40 is situated an epitaxial layer 3. Part of the epitaxial layer 3 is of the same conductivity type as, and has a higher resistivity than, the substrate 2 and forms with the substrate 2 and the collector region of the transistor; a diffused base region 4 and a diffused emitter
45 region 5, are present in the layer 3 as shown in Figure 1.

On one surface 6 of the semiconductor body 1 a conductive track 7,8 extends which
50 for the greater part of its length is secured to and insulated from the semiconductor body 1 by means of insulating material 9. The conductive track consists of two parts 7 and 8 which, at windows in the insulating material 9, contact the base region 4 and the
55 emitter region 5, respectively, of the transistor. Each of these parts 7 and 8 has a first and a second metal layer which are denoted by 7a, 8a and 7b, 8b, respectively, and which are connected together locally via
60 an interposed third metal layer 7c, 8c the metal of the third metal layer differing from that of the first and that of the second layer

and forming with the layers a stable low-ohmic junction.

The projection on the semiconductor surface 6 of the junction between the first metal layer 7a, 8a and the third metal layer 7c, 8c and that of the junction between the second metal layer 7b, 8b and the third metal layer
70 7c, 8c are juxtaposed.

In this manner a lateral separation between the first and the second metal layer is obtained as a result of which the metal of the second metal layer 7b, 8b cannot contact
75 directly the metal of the first metal layer 7a, 8a, not even through pin holes in the third metal layer 7c, 8c and particularly stable low-ohmic junctions are obtained. The junction between the first 7a, 8a and the third
80 7c, 8c and that between the second 7b, 8b and the third metal layer 7c, 8c are situated at least for the greater part on the same side of the third metal layer 7c, 8c.

The second metal layer 7b, and 8b, forms contact surfaces to which connection
85 conductors 10 and 11, for example, of gold are connected for connecting the base and the emitter of the transistor, to, for example, the gold-plated connection pins of a conventional envelope. The
90 collector is contacted via the substrate 2.

The transistor shown in Figure 1 can be manufactured entirely in a manner conventionally used in semiconductor technology.
95 After providing the base and emitter regions by diffusion, a layer of tungsten and then a layer of gold are provided on the insulating layer 9 which has no apertures therein, by successive vapour deposition in the same
100 vacuum. By conventional photolithographic and etching methods, a pattern is then obtained from said layers to form the second metal layer 7b, 8b of gold and the third
105 metal layer 7c, 8c of tungsten. Finally, apertures are provided in the insulating layer at the area of the emitter and the base regions and the first metal layer of, for example, aluminium is provided, the pattern of which
110 is defined by etching to form the parts 7a and 8a of the conductive track.

The transistor can be mounted in any conventional envelope in which the connection
115 conductors 10 and 11 are connected to the second metal layer 7b, 8b.

In the part of the second device shown in Figure 2, a conductive track secured to a semiconductor body 20 via an insulating layer
120 21, comprises a first metal layer 22 which is connected to a second metal layer 25 via an interposed third metal layer 24. The first metal layer 22, and a part of the third metal layer 24, are covered with a second insulating layer 26. The second metal layer 25 extends fully on the free surface of the uppermost
125 insulating layer 26. Via an aperture 27

in said layer 26, and via the third metal layer 24 the layer 25 is connected to the first metal layer 22. The layer 22 is situated substantially entirely between the two insulating layers 21 and 26.

The insulating layer 21, consists, for example, of thermal silicon dioxide, or another suitable insulator. On this layer, is provided, for example, a first metal layer 22 of aluminium from which a pattern is obtained by etching; the device is then provided with a third metal layer of nickel. In order to obtain a good low-ohmic junction between the aluminium and the nickel, it may be necessary to use an after-treatment at a slightly elevated temperature, and/or to provide a thin layer, of, for example, titanium, aluminium, or chromium between the aluminium and the nickel in order to reduce the oxide skin which is usually present on the aluminium.

The assembly may then be covered with the second insulating layer 26, for example, of silicon dioxide, provided by deposition from the vapour phase. In this layer an aperture 27 situated above the nickel is provided after which a layer 28 of, for example, nickel is vapour-deposited. This layer 28 can be locally reinforced by electro-deposition at an opening in a mask consisting of a layer of photo-lacquer so as to form the second metal layer 25, for example, of copper. The nickel layer 28 is used as the electrode during the reinforcement by electro-deposition and then a pattern may be obtained from said layer. Furthermore, the adherence of the copper layer to the insulating layer 26 is considerably improved by using the interposed nickel layer 28.

The reinforced parts forming the second metal layer 25 and projecting above the insulating layer 26 enable the device to be mounted on an insulating substrate which comprises conductive tracks, the surface 29 of the semiconductor body on which insulating material is present facing the said substrate. The layer 25 can be tin-plated and soldered in any conventional manner to the conductive tracks of the substrate.

It is to be noted that, although the reinforced second metal layer 25 in the present example is provided at the area of the aperture 27, it may also extend further over the insulating layer 26, in which case the layer 25 may have only locally reinforced portions for mounting the device.

The third device, a part of which is shown in Figure 3, comprises a semiconductor body 30 having an insulating layer 31 on which a first metal layer 32 of, for example, aluminium is present. Part 32 of the conductive track 32 to 34 serves for contacting and possible interconnection of semiconductor regions of semiconductor circuit elements of the semiconductor body 30, of which regions

only one is shown for reasons of clarity, namely the region 35.

The metal layer 32 adjoins, and forms a junction with, a third metal layer 33 which has comparatively small dimensions.

The metal layers 32 and 33 are covered with a second insulating layer 36, in which an aperture is present at part of the metal layer 33; at the said aperture, the second metal layer 34 situated substantially entirely on the free surface is connected to the third metal layer 33.

Both the junction between the first and third metal layers and the junction between the second and third metal layers are situated at least for the greater part on the side of the third metal layer 33 remote from the semiconductor body 30, said layer 33 extending entirely on the insulating layer 31 situated between the semiconductor surface 37 and the uppermost insulating layer 36. The material chosen for the third metal layer 33 is less apt to form an oxide skin than the first metal layer 32. The third metal layer is provided first and then the first metal layer, so that substantially no oxide will be present on the junction between the said layers so that the formation of a low-ohmic junction is facilitated.

Furthermore, the surface area of the junction between the second metal layer 34a, b and the third metal layer 33 is small relative to the overall surface area of the second metal layer, while the second metal layer 34 is at least locally thicker, namely at 34b, than the first metal layer 32 and projects laterally to beyond the semiconductor body 30.

In the present embodiment the first metal layer consists substantially entirely of aluminium and is approximately $1\text{ }\mu\text{m}$ thick. The second metal layer consists substantially entirely of gold and the projecting reinforced parts 34b thereof have a thickness of approximately $10\text{ }\mu\text{m}$. The part 34a of the second metal layer which is not reinforced and is used also for interconnection of circuit elements, has a thickness of approximately $1\text{ }\mu\text{m}$.

The third metal layer which preferably is substantially impermeable to the materials of the first and the second metal layers may consist of one of the metals platinum, nickel, tungsten and rhodium; in the present embodiment, the third metal layer consists of molybdenum and has a thickness of approximately $0.4\text{ }\mu\text{m}$ and lateral dimensions of approximately $35\text{ }\mu\text{m} \times 35\text{ }\mu\text{m}$.

In order to improve the ohmic contact between the first metal layer 32 and the semiconductor zone 35, materials may be used in the window, for example, platinum silicide, palladium silicide, and cobalt silicide, which materials provide a very stable and low-

ohmic contact, for example after alloying. A contact diffusion may also be performed.

The adherence between the metal layers and the insulating material may be improved, if desired, by using a thin layer of preferably titanium, chromium, molybdenum, niobium, cobalt or nickel. In the present embodiment, a thin layer 39 of titanium having a thickness of approximately 0.05 μm is used between the gold layer 34a, b and the insulating layer 36.

Such a semiconductor device can be manufactured entirely by techniques conventionally used in semiconductor technology. The aluminium layer 32 can be vapour-deposited, for example, or be obtained by RF sputtering, after which the excessive aluminium can be removed with conventional photolithographic and etching methods. The molybdenum layer 33 can be provided in a corresponding manner, for example, by means of RF or triode sputtering. The titanium layer 39 can be vapour-deposited and the gold layer 34 can be provided, for example, by vapour deposition and/or by electro-deposition. The second insulating layer 36 can be provided, for example, by sputtering, and has a thickness between 1 and 2 μm .

The semiconductor material below the projecting parts 34b can then be removed in any conventional manner in which, for example, a large number of devices which are manufactured in the same semiconductor wafer, can be severed simultaneously from each other by dividing the semiconductor wafer.

Many modifications are possible within the scope of the present invention defined in the appended Claims. The semiconductor body usually consists of silicon, but may be, for example, of germanium or an A_{III}B_V compound and may comprise, in addition to regions of bipolar transistors, other circuit elements, for example, field effect transistors, diodes, resistors and capacitors. The invention furthermore relates both to single circuit elements and to more complex devices, for example, integrated circuits. In particular, the embodiments of Figures 2 and 3 may be used both in devices in which the conductive track is provided at least mainly at one level, the level of the first metal layer, and in devices in which the conductive track is divided over two or more levels, for example, in connection with the complexity and the number of circuit elements of the device. Due to the presence of the second insulating layer 26, 36, for example, a second level for the conductive track is already present in which the conductive track on said second or uppermost level may consist fully or partly of the same material as the second metal layer.

Instead of silicon dioxide other insulating materials may be used, for example, silicon nitride, aluminium oxide, or a combination

of insulating materials; in the latter case, for example, the track can be oxidized partly to form the insulating material.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body on a surface of which extends a conductive track which is secured to and insulated from the semiconductor body over at least part of its length by means of an insulating material, said conductive track comprising first and second metal layers of different materials which are connected locally via an interposed third metal layer, the material of the third metal layer differing from that of the first and that of the second metal layers and forming therewith stable low-ohmic junctions, the projections on the semiconductor body surface of the junctions between the first and third metal layers and the second and third metal layers being juxtaposed.

2. A semiconductor device as claimed in Claim 1 wherein the semiconductor body comprises two or more regions of opposite conductivity types associated with a semiconductor circuit element, at least one of the said regions being connected to the first metal layer at an aperture in the insulating material, the second metal layer being provided with a connection conductor.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein a plurality of layers of insulating material are present at the surface of the semiconductor body, the second metal layer extending substantially entirely on the free surface of the uppermost insulating layer and being connected via at least one aperture in the uppermost insulating layer and via the third metal layer to the first metal layer which is situated substantially entirely between two of said insulating layers.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the surface area of the junction between the second and the third metal layer is small compared with the overall surface area of the second metal layer.

5. A semiconductor device as claimed in any of the preceding Claims, wherein the junction between the first and third metal layers and that between the second and third metal layers are situated, at least for the greater part, on the same side of the third metal layer.

6. A semiconductor device as claimed in Claims 4 and 5, wherein the two junctions are situated, at least for the greater part, on the side of the third metal layer remote from the semiconductor body, the third metal layer extending entirely on an insulating layer situated between the semiconductor surface and the uppermost insulating layer.

7. A semiconductor device as claimed in any of the preceding Claims, wherein the conductive track comprises at least one part

ohmic contact, for example after alloying. A contact diffusion may also be performed.

The adherence between the metal layers and the insulating material may be improved, if desired, by using a thin layer of preferably titanium, chromium, molybdenum, niobium, cobalt or nickel. In the present embodiment, a thin layer 39 of titanium having a thickness of approximately $0.05\ \mu\text{m}$ is used between the gold layer 34a, b and the insulating layer 36.

Such a semiconductor device can be manufactured entirely by techniques conventionally used in semiconductor technology. The aluminium layer 32 can be vapour-deposited, for example, or be obtained by RF sputtering, after which the excessive aluminium can be removed with conventional photolithographic and etching methods. The molybdenum layer 33 can be provided in a corresponding manner, for example, by means of RF or triode sputtering. The titanium layer 39 can be vapour-deposited and the gold layer 34 can be provided, for example, by vapour deposition and/or by electro-deposition. The second insulating layer 36 can be provided, for example, by sputtering, and has a thickness between 1 and $2\ \mu\text{m}$.

The semiconductor material below the projecting parts 34b can then be removed in any conventional manner in which, for example, a large number of devices which are manufactured in the same semiconductor wafer, can be severed simultaneously from each other by dividing the semiconductor wafer.

Many modifications are possible within the scope of the present invention defined in the appended Claims. The semiconductor body usually consists of silicon, but may be, for example, of germanium or an A_{1-x}B_x compound and may comprise, in addition to regions of bipolar transistors, other circuit elements, for example, field effect transistors, diodes, resistors and capacitors. The invention furthermore relates both to single circuit elements and to more complex devices, for example, integrated circuits. In particular, the embodiments of Figures 2 and 3 may be used both in devices in which the conductive track is provided at least mainly at one level, the level of the first metal layer, and in devices in which the conductive track is divided over two or more levels, for example, in connection with the complexity and the number of circuit elements of the device. Due to the presence of the second insulating layer 26, 36, for example, a second level for the conductive track is already present in which the conductive track on said second or uppermost level may consist fully or partly of the same material as the second metal layer.

Instead of silicon dioxide other insulating materials may be used, for example, silicon nitride, aluminium oxide, or a combination

of insulating materials; in the latter case, for example, the track can be oxidized partly to form the insulating material.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body on a surface of which extends a conductive track which is secured to and insulated from the semiconductor body over at least part of its length by means of an insulating material, said conductive track comprising first and second metal layers of different materials which are connected locally via an interposed third metal layer, the material of the third metal layer differing from that of the first and that of the second metal layers and forming therewith stable low-ohmic junctions, the projections on the semiconductor body surface of the junctions between the first and third metal layers and the second and third metal layers being juxtaposed.

2. A semiconductor device as claimed in Claim 1 wherein the semiconductor body comprises two or more regions of opposite conductivity types associated with a semiconductor circuit element, at least one of the said regions being connected to the first metal layer at an aperture in the insulating material, the second metal layer being provided with a connection conductor.

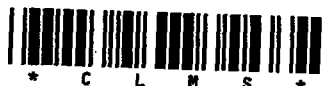
3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein a plurality of layers of insulating material are present at the surface of the semiconductor body, the second metal layer extending substantially entirely on the free surface of the uppermost insulating layer and being connected via at least one aperture in the uppermost insulating layer and via the third metal layer to the first metal layer which is situated substantially entirely between two of said insulating layers.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the surface area of the junction between the second and the third metal layer is small compared with the overall surface area of the second metal layer.

5. A semiconductor device as claimed in any of the preceding Claims, wherein the junction between the first and third metal layers and that between the second and third metal layers are situated, at least for the greater part, on the same side of the third metal layer.

6. A semiconductor device as claimed in Claims 4 and 5, wherein the two junctions are situated, at least for the greater part, on the side of the third metal layer remote from the semiconductor body, the third metal layer extending entirely on an insulating layer situated between the semiconductor surface and the uppermost insulating layer.

7. A semiconductor device as claimed in any of the preceding Claims, wherein the conductive track comprises at least one part



which is associated with the second metal layer, is thicker than the first metal layer and projects laterally beyond the semiconductor body.

5 8. A semiconductor device as claimed in any of the preceding Claims, wherein the first metal layer consists substantially entirely of aluminium.

10 9. A semiconductor device as claimed in any of the preceding Claims, wherein the second metal layer consists substantially entirely of gold.

15 10. A semiconductor device as claimed in any of the preceding Claims, wherein the third metal layer consists substantially entirely of a metal belonging to the group consisting of molybdenum, platinum, nickel, tungsten and rhodium.

20 11. A semiconductor device as claimed in any of the preceding Claims, wherein a thin

layer of a material which belongs to the group consisting of titanium, chromium, molybdenum, niobium, cobalt and nickel, is situated between at least one of the metal layers and the insulating material.

12. A semiconductor device substantially as herein described with reference to Figure 1 of the accompanying drawing.

13. A semiconductor device substantially as herein described with reference to Figure 2 of the accompanying drawing.

14. A semiconductor device substantially as herein described with reference to Figure 3 of the accompanying drawing.

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