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DOT PRODUCT CIRCUIT FOR MULTIPATH RECEIVERS

BACKGROUND OF THE INVENTION

5 I. Field of the Invention

The present invention relates to communication systems. More particularly, the present invention relates to a novel and improved method and apparatus for demodulating a communication signal by generating a dot product between a pilot signal and a data signal contained within said communication signal.

II. Description of the Related Art

15 In communication systems in which digital signals are transmitted, various demodulation schemes exist for the extraction of the data from the received signals. In particular, systems which use quadrature phase shift keyed (QPSK) modulation techniques do not readily permit, upon demodulation of the received signal, the extraction of information necessary to accomplish signal weighting for multipath signal combining.

It is therefore an object of the present invention to provide for in the demodulation of a modulated signal a weighting process with respect to a received reference.

25 SUMMARY OF THE INVENTION

The present invention is a novel and improved method and apparatus for, in a communication system in which digital data is digitally modulated and transmitted, demodulating the transmitted signals for extracting the transmitted digital data. More specifically, the present invention is employed in a digital communication system in which a data signal data along with a pilot signal are both bi-phase shift keyed modulated and quadrature phase shift keyed (QPSK) spread upon a carrier. At the receiver the data is extracted from the received signal by computing a dot product between the pilot and data vectors. The magnitude of the component of the data vector that is in phase with the pilot vector, a phase reference for the data, is determined by the dot product of these vectors. In



BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when
5 taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

Figure 1 is an exemplary block diagram of a receiver implementing the dot product processing of the present invention;

10 Figure 2 is an exemplary vector representation of received pilot and data signals;

Figure 3 is an exemplary block diagram of the digital receive and associated circuitry for extracting pilot and information data from the received I and Q signal components;

Figure 4 is an exemplary diagram of the QPSK signal space;

15 Figure 5 is a functional block diagram of the dot product circuits of Figure 3; and

Figure 6 is a block diagram illustrating an exemplary implementation of the dot product circuits of Figure 3.

20 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In U.S. Patent No. 5,103,459 entitled "SYSTEM AND METHOD FOR FORMING SIGNAL WAVEFORMS IN A CDMA CELLULAR
25 TELEPHONE SYSTEM", assigned to the Assignee hereof and of which the disclosure is incorporated by reference, a modulation scheme is disclosed for the transmission of digitally modulated signals. This modulation scheme uses in the cell-to-mobile link a pilot signal that is transmitted along with data signals for use as a phase reference by the receiving
30 demodulator. The use of a pilot signal for this purpose is well known and is further disclosed in U.S. Patent No. 4,901,307 entitled "SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS", also assigned to the Assignee hereof and of which the disclosure is incorporated by reference.

35 A receiver is disclosed in the above mentioned U.S. Patent No. 5,103,459 for demodulation of the transmitted QPSK spread pilot and data



Figure 2 illustrates an exemplary vector representation of a pilot signal and a data signal. In Figure 2, the despread I and Q components of the pilot signal and data signal for one finger of the diversity RAKE receiver respectively define pilot signal vector 20 and data signal vector 22 in the IQ constellation. The pilot signal is typically transmitted at a greater signal strength than the data signals, and as such the magnitude of pilot signal vector 20 is greater than a received data signal vector 22. Furthermore, since the pilot signal vector is much stronger than the data signal vector it can be used as an accurate phase reference for signal processing.

In the transmission process the pilot and data signals as transmitted travel the same path to the receiver. In the absence of noise the pilot and data vectors coincide and are at a phase angle of one of $\pi/4$, $-\pi/4$, $3\pi/4$ or $-3\pi/4$. However due to channel noise the received signal may be offset from the transmitted phase angle. In the exemplary embodiment of the present invention the pilot signal is further low pass filtered to remove noise and data, while the data signal remains unfiltered. Thus when noise exists a phase difference of θ will result between the pilot and data vector with the pilot serving as an accurate phase reference. It should be noted that the vectors as illustrated in Figure 2 a phase difference is shown to exist between the pilot and data vectors.

The formulation of the dot product, also known as the scalar product of pilot signal vector 20 and data signal vector 22 is particularly advantageous in extracting the data from the received signal in a multiple demodulator or multi-finger diversity receiver. In this type of receiver the several fingers are assigned to demodulated signals from several different paths or sources. Within each finger the dot product is used to find the magnitude of the component of the data vector that is in phase with the pilot vector by projecting the data vector onto the pilot vector. In forming a dot product between the pilot and data vector orthogonal noise on the data is removed.

In the multi-finger diversity receiver the dot product for data produced by each finger also serves to weight the data for efficient combining. Thus the dot product serves to scale the data by the magnitude of the pilot signal before combining. If none of the input signals are orthogonal to the data, and the total input power is kept at a set point, the



PN sequences PN_I and PN_Q . Pilot PN sequence generator 32 generates the PN sequences PN_I and PN_Q identical to those used in the transmitter according to sequence timing and state input (not shown) as provided from controller 18 (Figure 1). Controller 18 is typically implemented as a microprocessor and includes the appropriate memory and program instructions.

In the exemplary embodiment I and Q component signal samples are provided to QPSK despreader 30 at a sample rate which corresponds to the eight times the chip rate of the PN sequences. However it should be understood that the samples may be provided at any other rate at or greater than the PN sequence chip rate. In the exemplary embodiment the PN chip rate is 1.2288 Mcps which is much greater than the data symbol rate of 19.2 kbps.

QPSK despreader 30 strips off the PN spreading on the composite I and Q component signal samples so as to extract therefrom composite I and Q component samples. In order to understand the operation of despreader 30 it is necessary to understand the effect the exemplary transmission modulation scheme, BPSK modulation and QPSK spreading, has upon the pilot and data signals. Figure 4 illustrates the modulation constellation for I and Q spread signals. A BPSK signal is normally transmitted using no phase shift or a phase shift of 180° in the carrier to represent the two data states, i.e., "0" or a "1". In providing two versions of the same data bit for QPSK spreading in the BPSK modulation scheme where there is no I or Q spreading signal input, the I/Q output signal is of the signal space coordinates (0,0) or (1,1). With the contribution from the I and Q PN sequences in the QPSK spreading the resultant signal is of one of four phase as illustrated in Figure 4. Table I below illustrates the correspondence between the data occurring at the coordinates (0,0) or (1,1) and the counter-clockwise rotation as a result of the I and Q spreading.

TABLE I

I PN	Q PN	ANGLE OF ROTATION
0	0	0°
0	1	270°
1	0	90°
1	1	180°



34 and 36 are samples of the I and Q components of the pilot signal and are referred to as Pilot I (P_I) and Pilot Q (P_Q) samples. The Pilot I and Pilot Q samples are provided to dot product circuit 38 which is part of digital circuitry 16 (Figure 1).

5 It should be understood that in the modulation scheme considered for this example the pilot signal transmitted uses the all-zero Walsh code as the pilot signal which is PN spread by the I and Q PN spreading sequences. In using the all-zero Walsh code the PN spread pilot signal is the same as the I and Q PN spreading sequences themselves. Therefore by
10 removing the PN spreading on the composite I and Q component signal, and filtering, the all-zero pilot is recovered. It should be understood that any other one of the Walsh codes may be used as the pilot signal. It should be further understood that for the pilot signal a predetermined input may be covered by a Walsh sequence for transmission. Upon
15 reception the Walsh covering is removed from the despread signal, in a manner as described below with respect to data recovery, so as to recover the original input.

In order to recover the data, I and Q components are also respectively output from QPSK despreaders 30 to digital mixers 40 and 42
20 which may be configured as modulo-two adders or exclusive-or gates. Digital mixers 40 and 42 also receive from Walsh sequence generator 44 a Walsh sequence. This Walsh sequence is identical to the Walsh sequence assigned to this channel in the transmitter and is selected in accordance with a sequence assignment input (not shown) from controller 18. In the
25 exemplary embodiment the Walsh sequence chip rate is also 1.2288 Mcps. Digital mixers 40 and 42 perform a modulo-2 addition between the Walsh chip and the respectively input I and Q components samples. The despread and now uncovered I and Q component samples are output from digital mixers 40 and 42 where they are respectively provided to
30 accumulators 46 and 48. Accumulators 46 and 48 respectively accumulate the I and Q component samples over a symbol time, which in the exemplary embodiment corresponds to 64 samples or 1/19200 second. The output from accumulators 46 and 48 are at the symbol rate of 19200 symbols/second and are the respective symbol data I and Q, referred to
35 herein as Data I (D_I) and Data Q (D_Q) samples. The Data I and Data Q samples are also provided to dot product circuit 38. Accumulators 46



of the multiplication in multiplier 72 between the Data Q sample and the Pilot Q sample are provided as another input to digital adder 74. Adder 74 sums the two input values to provide an output symbol sample for combining with demodulated symbols from other paths. The value of this symbol sample represents the value of the data vector in phase with the pilot vector scaled by the pilot signal strength.

Figure 6 provides an exemplary implementation of dot product circuit 38 of Figure 3, with dot product circuit 50 and 52 being of identical construction. The circuit of Figure 6 implements in digital circuit form equations (1) and (2) set forth above. In Figure 6, Data I and Data Q samples, and the corresponding Pilot I and Pilot Q samples are respectively provided to latches 80, 82, 84 and 86 where they are stored in response to a latch enable signal provided at the symbol rate. Since each of these samples are multiple-bit samples, each of latches 80 - 86 are constructed as a series of latch elements (not shown) each for storing a different bit of the sample.

The I,Q values stored in each of latches 80 and 82 are respectively provided to an I and a Q input of two-to-one (2:1) multi-bit input multiplexer 88. Similarly, the output of each of latches 84 and 86 are provided respectively to an I and a Q input of two-to-one (2:1) multi-bit input multiplexer 90. Also provided to multiplexers 88 and 90 is an I/Q select signal. Multiplexers 88 and 90 are responsive to the I/Q select signal for providing for half of the symbol period an output from one of the inputs, e.g., the I input, and for the other half of the symbol period an output from the other one of the inputs, e.g., the Q input.

The selected data and pilot samples output from multiplexers 88 and 90 are provided to serial multiply-and-accumulate element 92 which is comprised of digital multiplier 94 and accumulator 96. Element 92 for each symbol period sequentially multiplies in multiplier 94 the Data I sample with the Pilot I sample, multiplies in multiplier 94 the Data Q sample with the Pilot Q sample, and sums the product of these multiplication in accumulator 96 to provide the symbol sample value representative of the magnitude of the symbol in phase with the pilot. The value generated in element 92 is cleared from therein every symbol period in response to a symbol clock input.





CLAIMS

1. An apparatus for computing a scalar projection of a vector
2 onto another vector comprising:
means for multiplying a value representative of a first component
4 of a first vector with a value representative of a first component of a
second vector to provide a first intermediate value, and for multiplying a
6 value representative of a second component of a first vector with a value
representative of a second component of a second vector to provide a
8 second intermediate value; and
means for summing said first and second intermediate values and
10 providing a resultant value.
2. The apparatus of Claim 1 further comprising:
2 means for storing said values representative of said first and second
components of said first vector, and said values representative of said first
4 and second components of said second vector ; and
means responsive to a first state of a select signal for providing said
6 values representative of said first components of said first and second
vectors to said means for multiplying, and responsive to a second state of
8 said select signal for providing said values representative of said second
components of said first and second vectors to said means for multiplying.
3. The apparatus of Claim 1 wherein said means for
2 multiplying comprises:
a first multiplier having a pair of inputs for respectively receiving
4 said first vector first component and said second vector first component,
and an output coupled to said means for summing; and
6 a second multiplier having a pair of inputs for respectively
receiving said first vector second component and said second vector
8 second component, and an output.
4. The apparatus of Claim 3 wherein said means for summing
2 comprises an adder having a pair of inputs respectively coupled to said
first and second multiplier outputs, and an output.
5. In a communication system receiver which receives a pilot
2 signal and a data signal each defining respective vectors and travelling a





input said data signal I component sample, said data signal Q component sample, said pilot signal I component sample and said pilot signal Q component sample;

8 a first digital multiplexer having a first multiplexer select signal input, a pair of first multiplexer sample inputs respectively coupled to said first and second latch sample outputs and a first multiplexer sample output coupled to said multiplier first input; and

12 a second digital multiplexer having a second multiplexer select signal input, a pair of second multiplexer sample inputs respectively coupled to said third and fourth latch sample outputs and a second multiplexer sample output coupled to said multiplier second input.

9. In a communication system receiver which receives a pilot signal and a data signal each defining respective vectors, each vector represented by I and Q components, an method for determining the magnitude of said data signal vector in phase with said pilot signal vector comprising the steps of:

6 multiplying said received data signal I component sample and pilot signal I component sample to provide a resultant first product sample;

8 multiplying said received data signal Q component sample and pilot signal Q component sample to provide a resultant second product sample; and

-10 summing said first and second product samples to provide a resultant sum sample of a value representative of the magnitude of said data signal vector in phase with said pilot signal vector.

10. The method of Claim 9 further comprising the steps of:

2 storing each of said data signal I component sample, said data signal Q component sample, said pilot signal I component sample and said pilot signal Q component sample;

4 providing said stored data signal I and pilot signal I component samples for multiplication thereof; and

6 providing said stored data signal Q and pilot signal Q component samples for multiplication thereof.

