ABSTRACT

A NEW METHOD TO PREVENT SIDE DAMAGE OF METAL DURING VIA ETCH

A new method of preventing via failure caused by misalignment to a metal line by forming conductive spacers on the metal line is described. Semiconductor device structures in and on a semiconductor substrate and covered with an insulating layer. Metal lines are formed overlying the insulating layer. Conductive spacers of titanium or titanium nitride are formed on the sidewalls of said metal lines. An intermetal dielectric layer is deposited over the metal lines. Via openings are etched through the intermetal dielectric layer to the metal lines wherein there is a misalignment of the via openings to the metal lines and wherein an edge of the metal lines is exposed by the misalignment. A barrier layer is deposited within the via openings and does not cover the exposed edge of the metal lines. A tungsten layer is dpeosited within the via openings using WF_6 gas to form metal plugs. The conductive spacers protect the exposed edge of the metal lines thereby preventing attack of the metal lines by fluorine ions. This completes fabrication of the integrated circuit without via failure.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)